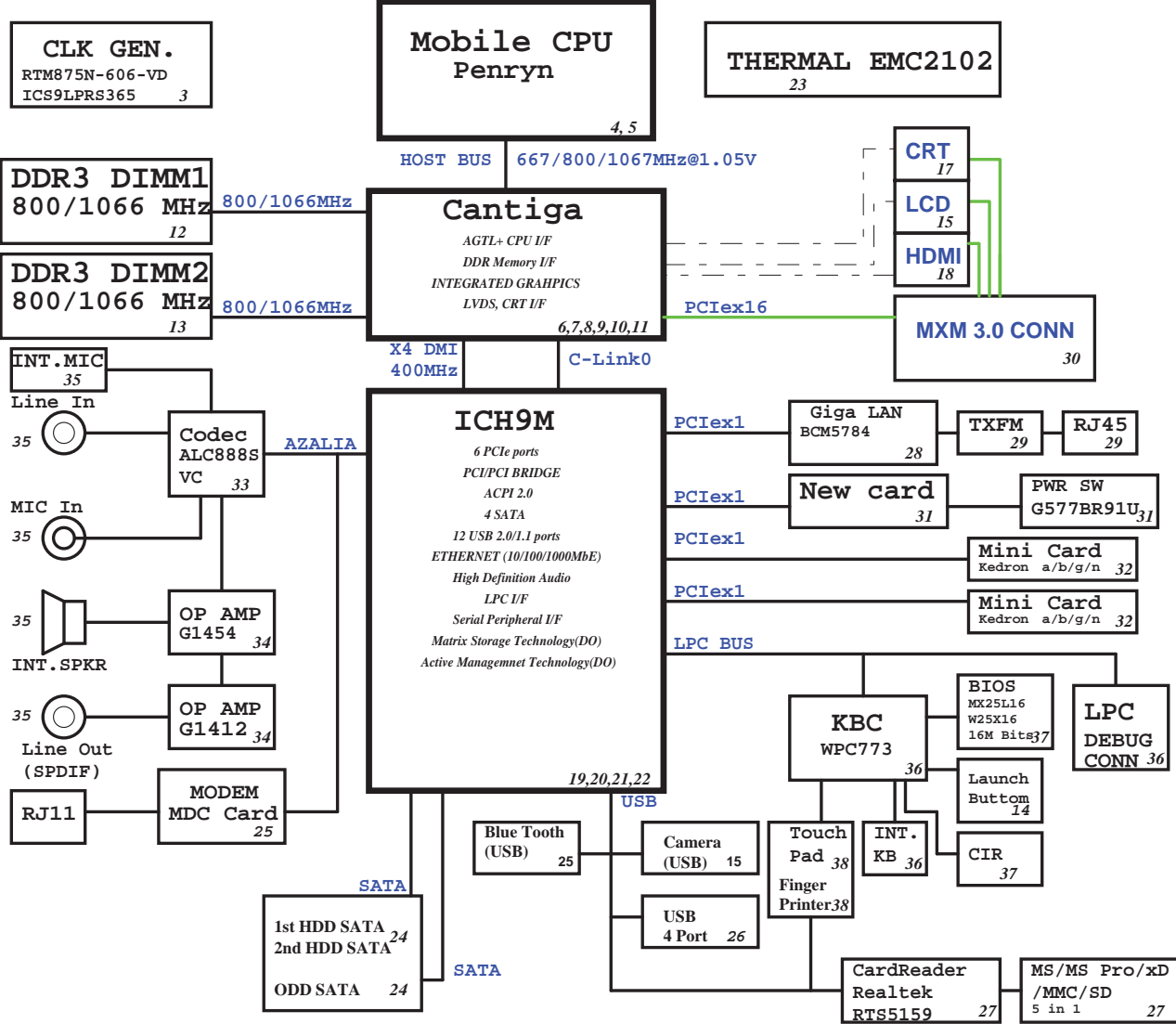
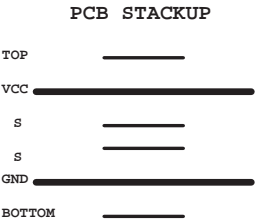


SJM80_MV/JV80_MV Block Diagram



Project code: 91.4DW01.001
PCB P/N : 48.4DW01.0SB
REVISION : 09221 -1



SYSTEM DC/DC TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D5V_S3

RT9026 44	
1D5V_S3	DDR_VREF_S3 DDR_VREF_S3_1

AO4468 44	
1D5V_S3	1D5V_S0

GFXCORE DC/DC ISL6263A 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER MAX8731A 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSFPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

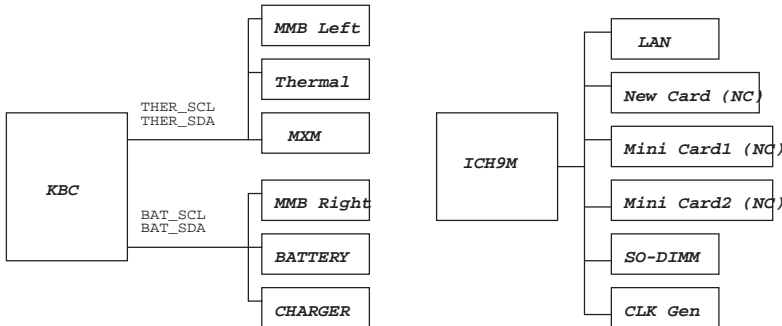
USB Table

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINI1 (WL)
4	CCD
5	NEW CARD
6	FP
7	BT
8	NC
9	USB1
10	MINI2
11	CARD READER

PCIE Routing

LANE1	LAN Broadcom 5784
LANE2	MiniCard WLAN
LANE3	MiniCard TV
LANE4	NC
LANE5	NewCard
LANE6	NC

SMBus



SJM80 UMA ONLY SB

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Reference	
Size A3	Document Number
SJM80/JV80	
Date: Monday, May 25, 2009	Rev -1
Sheet 2	of 51

6 H_A#(35..3) <<>>

CPU1A1 OF 4

H_A#3 J4
H_A#4 L5
H_A#5 L4
H_A#6 K5
H_A#7 M3
H_A#8 N2
H_A#9 J1
H_A#10 N3
H_A#11 P5
H_A#12 L2
H_A#13 L2
H_A#14 P4
H_A#15 P1
H_A#16 R1
M1C

6 H_ADSTB#0 <<>>
6 H_REQ#(4..0) <<>>

H_REQ#0 K3
H_REQ#1 H2
H_REQ#2 K2
H_REQ#3 J3
H_REQ#4 L1

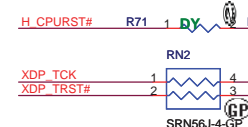
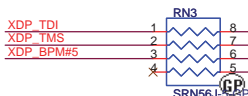
H_A#17 Y2
H_A#18 U5
H_A#19 R3
H_A#20 W6
H_A#21 U4
H_A#22 Y5
H_A#23 U1
H_A#24 R4
H_A#25 T5
H_A#26 T3
H_A#27 W2
H_A#28 W5
H_A#29 Y4
H_A#30 U2
H_A#31 V4
H_A#32 W3
H_A#33 AA4
H_A#34 AB2
H_A#35 AA3
V1

6 H_ADSTB#1 <<>>
19 H_A20M# <<>>
19 H_FERR# <<>>
19 H_IGNNE# <<>>
19 H_STPCLK# <<>>
19 H_INTR# <<>>
19 H_NMI# <<>>
19 H_SMI# <<>>

A6
A5
C4
D5
C6
B4
A3
SMI#

RSVD#M4
RSVD#N5
RSVD#T2
RSVD#V3
RSVD#B2
RSVD#B2
RSVD#D2
RSVD#D2
RSVD#D3
RSVD#F6
KEY_NC

BGA479-SKT6-GPU7
62.10079.001
62.10053.401



All place within 2" to CPU

ADDR GROUP 0
CONTROL

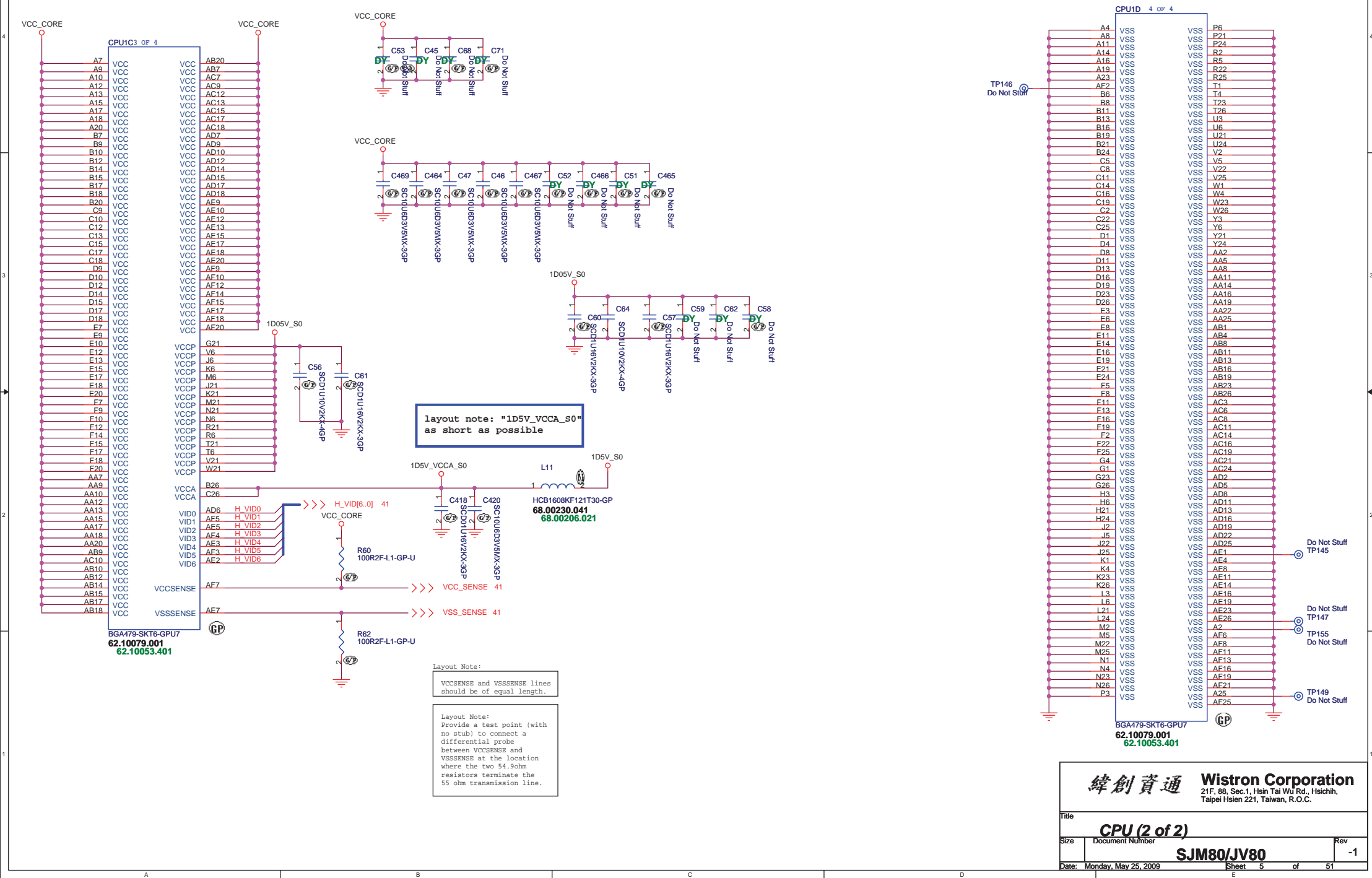
ADDR GROUP 1
STANDBY/SLP/ICP

ICP

RESERVED

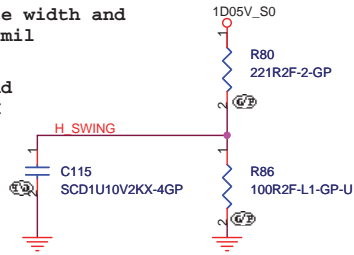
KEY_NC

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H_SWING routing Trace width and
Spacing use 10 / 20 mil

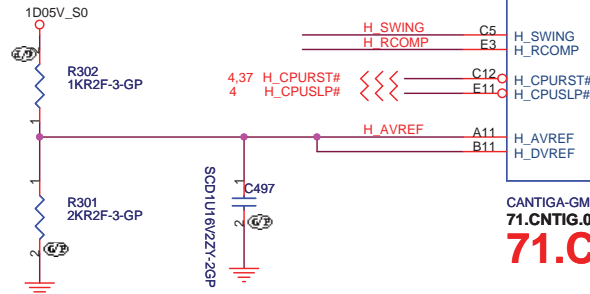
H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)



H_RCOMP routing Trace width and
Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



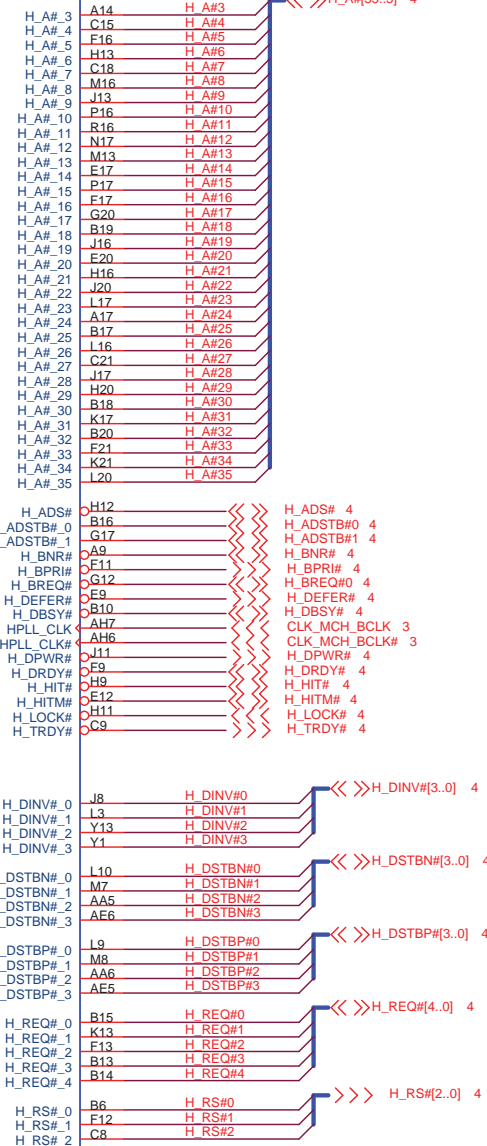
NB1A

1 OF 10

HOST

CANTIGA-GM-GP-U-NF
71.CNTIG.00U

71.CNTIG.D1U

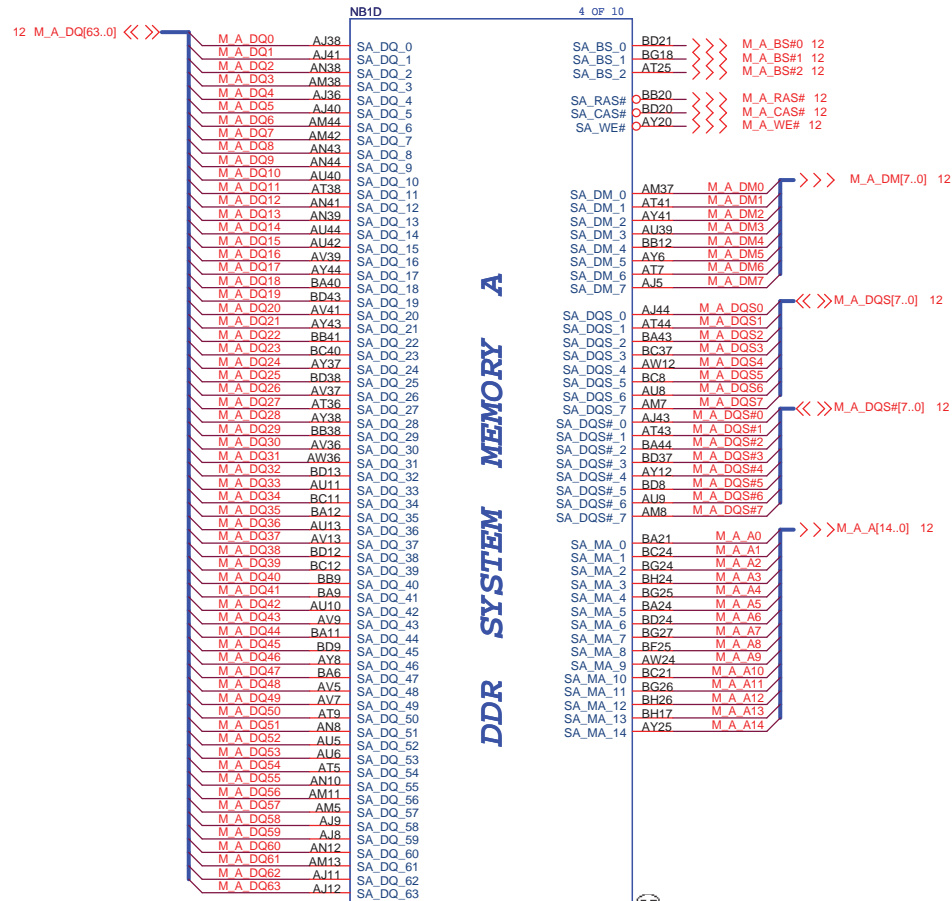


SJM80 UMA ONLY SB

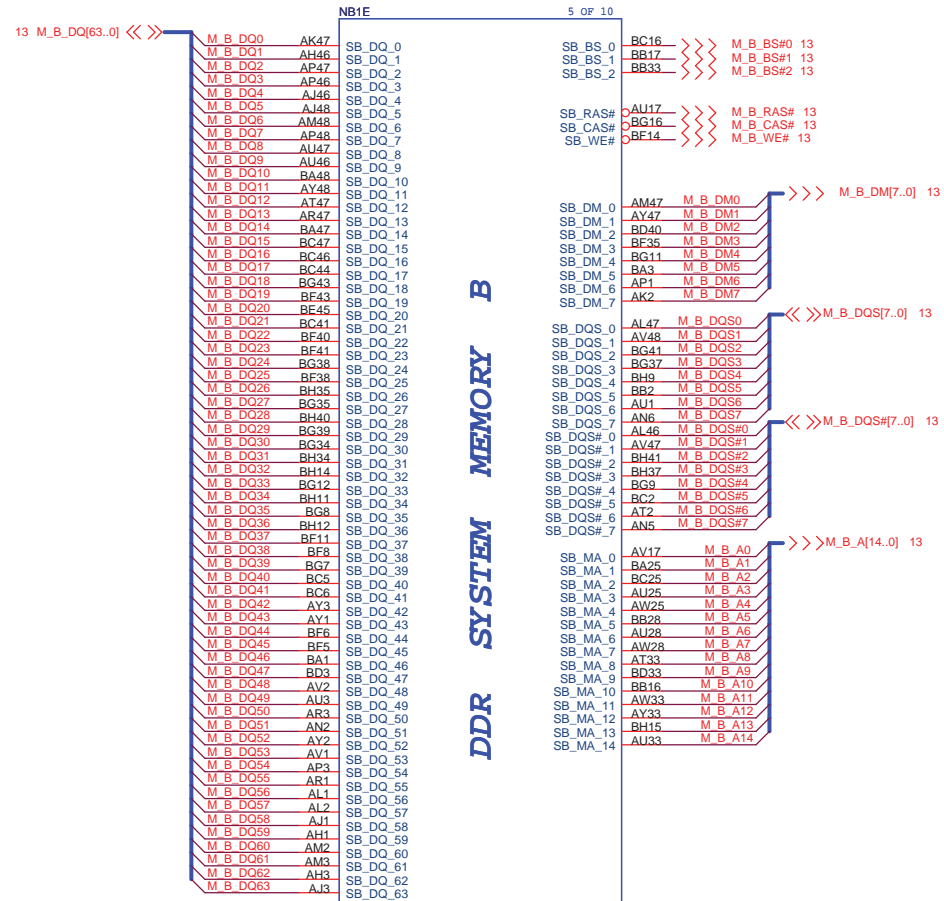
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Cantiga (1 of 6)	
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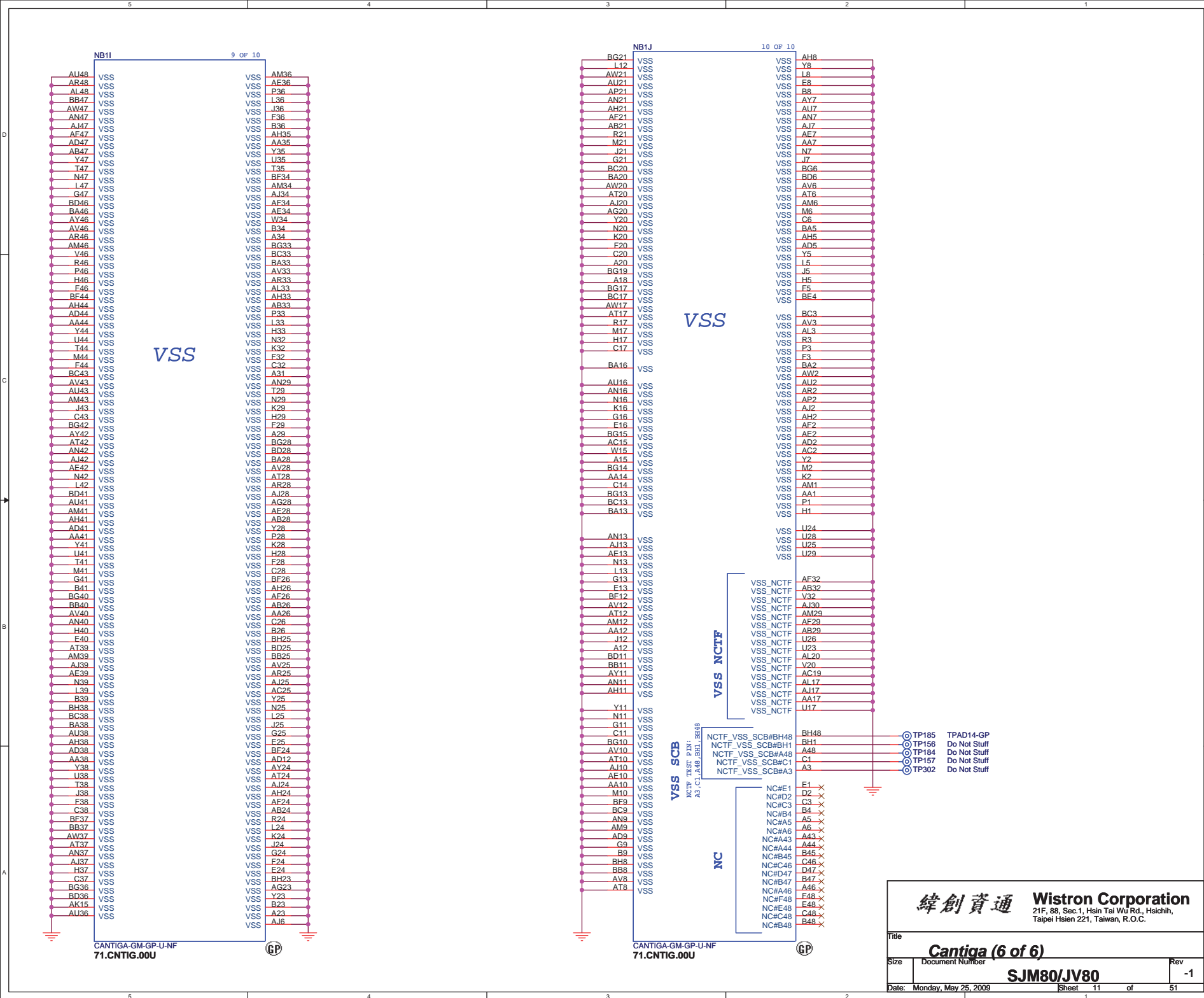


CANTIGA-GM-GP-U-NF
71.CNTIG.00U

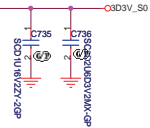
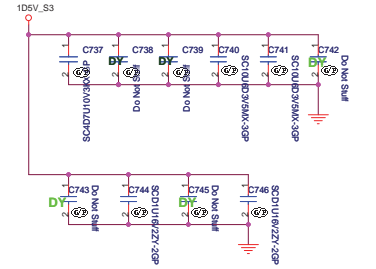
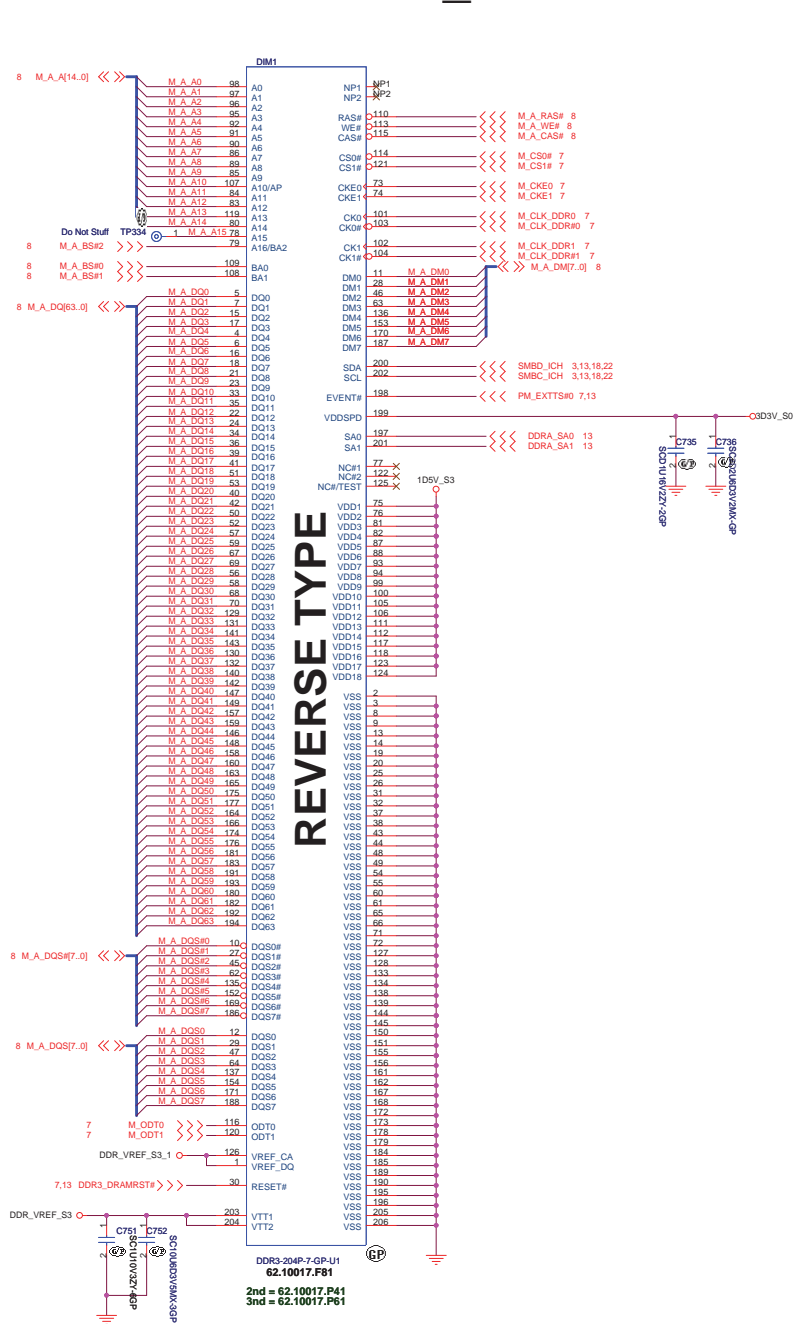


CANTIGA-GM-GP-U-NF
71.CNTIG.00U

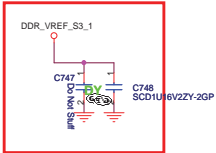
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Cantiga (3 of 6)	
Size	Document Number
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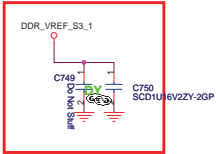
DDR3 SOCKET_1



Layout Note : Near Pin 126

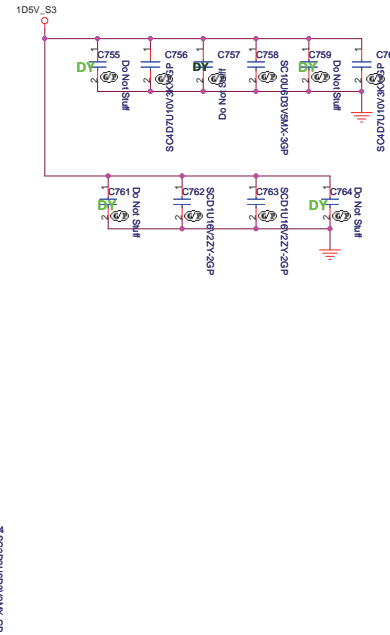
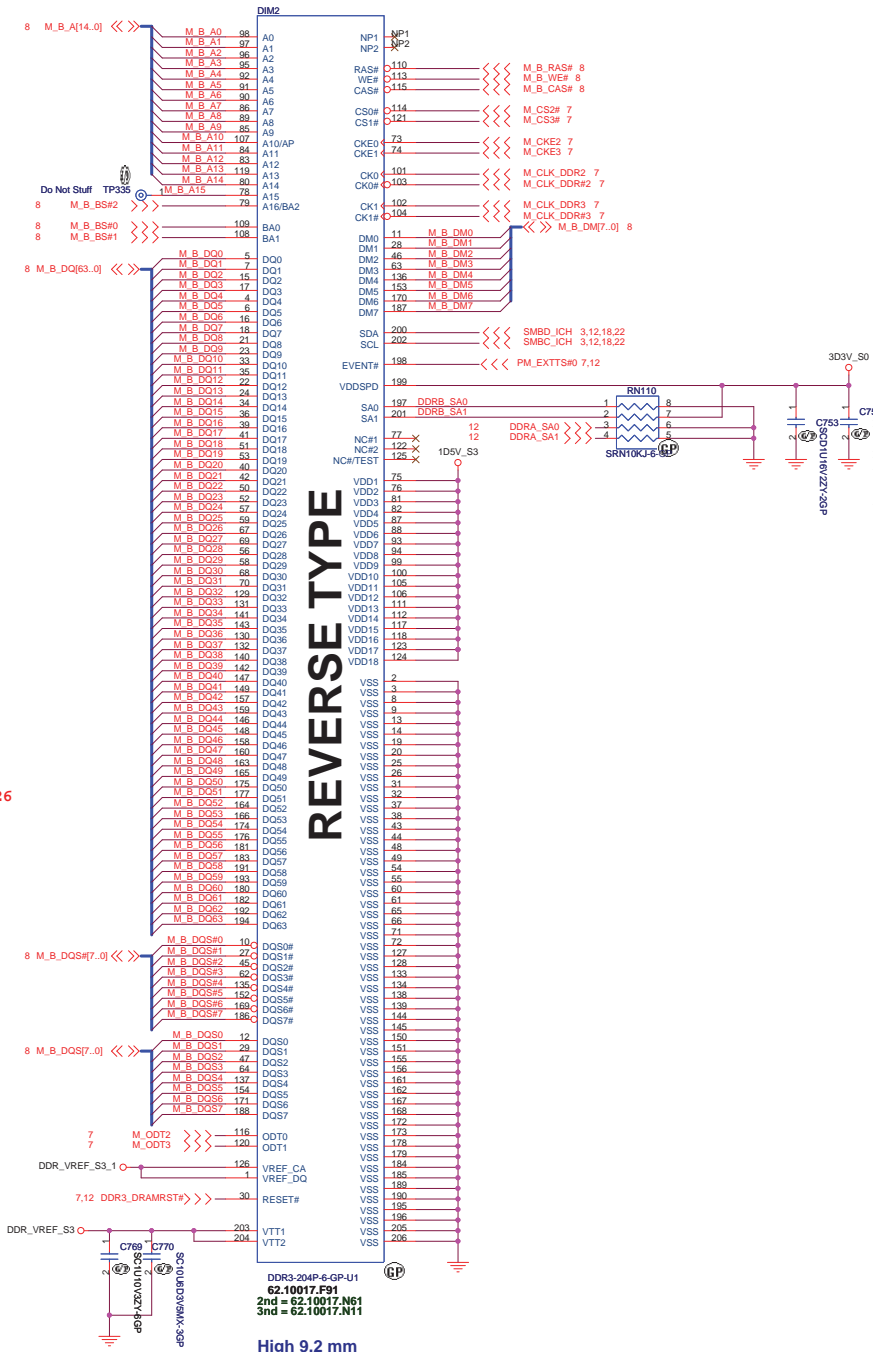


Layout Note : Near Pin 1

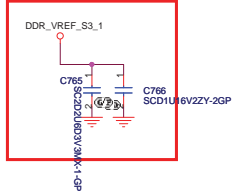


High 5.2mm

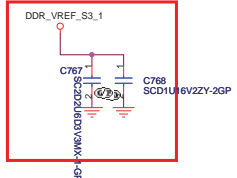
DDR3 SOCKET_2



Layout Note : Near Pin 126



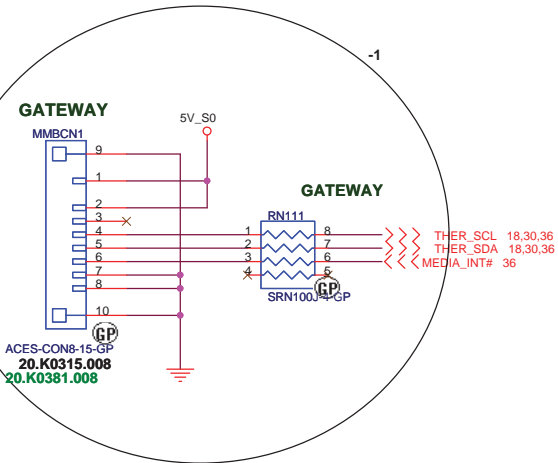
Layout Note : Near Pin 1



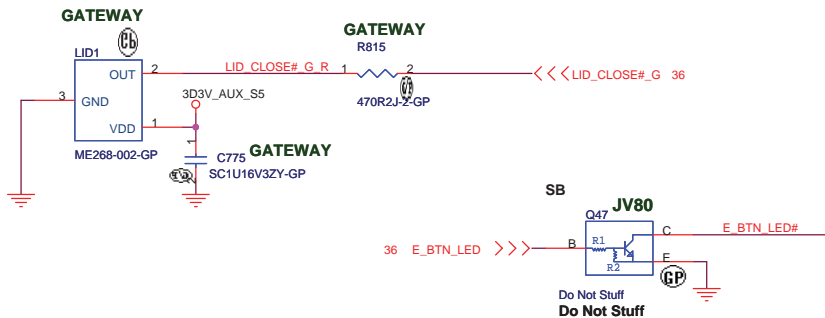
DDR3-204P-6-GP-U1
62.10017.F91
2nd = 62.10017.N61
3rd = 62.10017.N11

High 9.2 mm

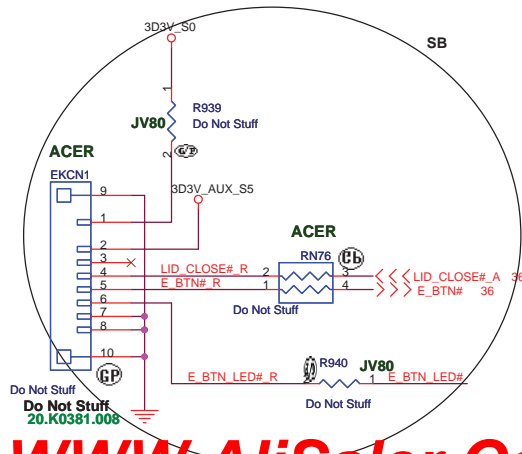
MMB Lounch For GATEWAY



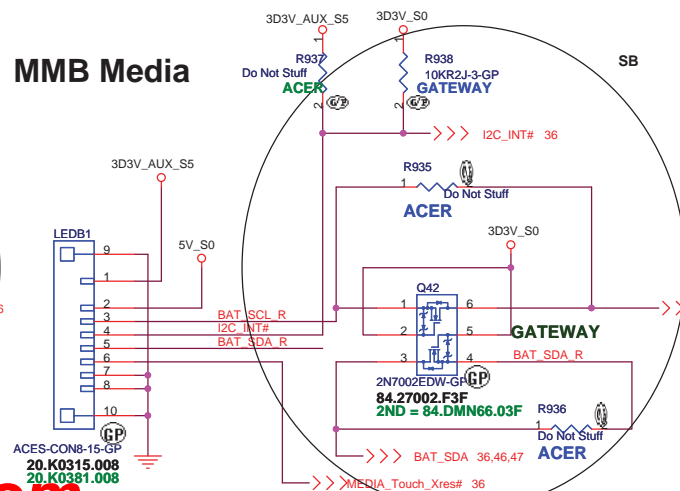
LID SWITCH



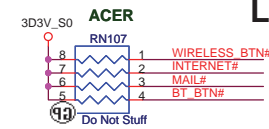
E-KEY Button



MMB Media

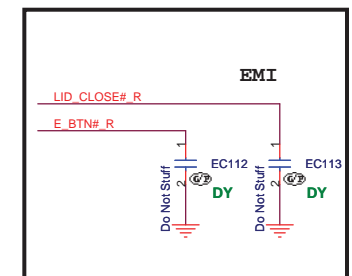
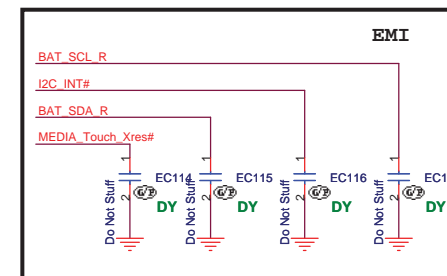
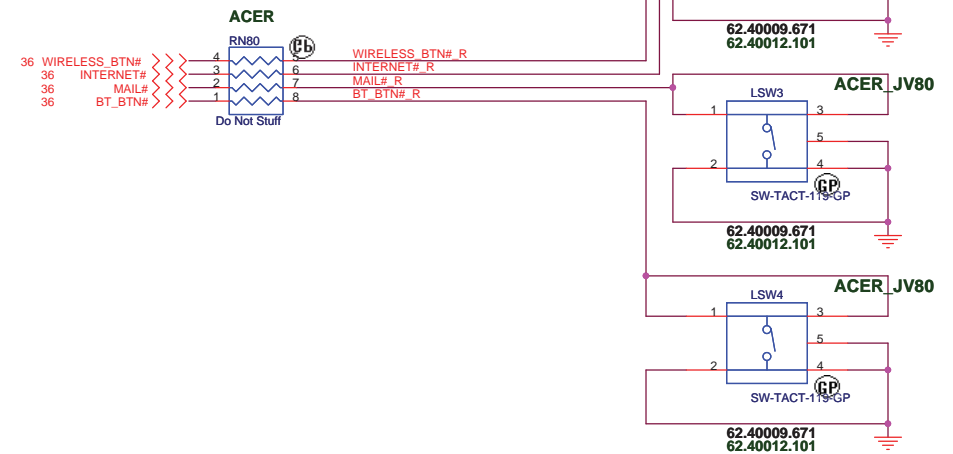


LAUNCH Button



JV80_MV change Function

Internet ==> BlueTooth
Mail ==> Backup
BlueTooth ==> TouchPad Lock

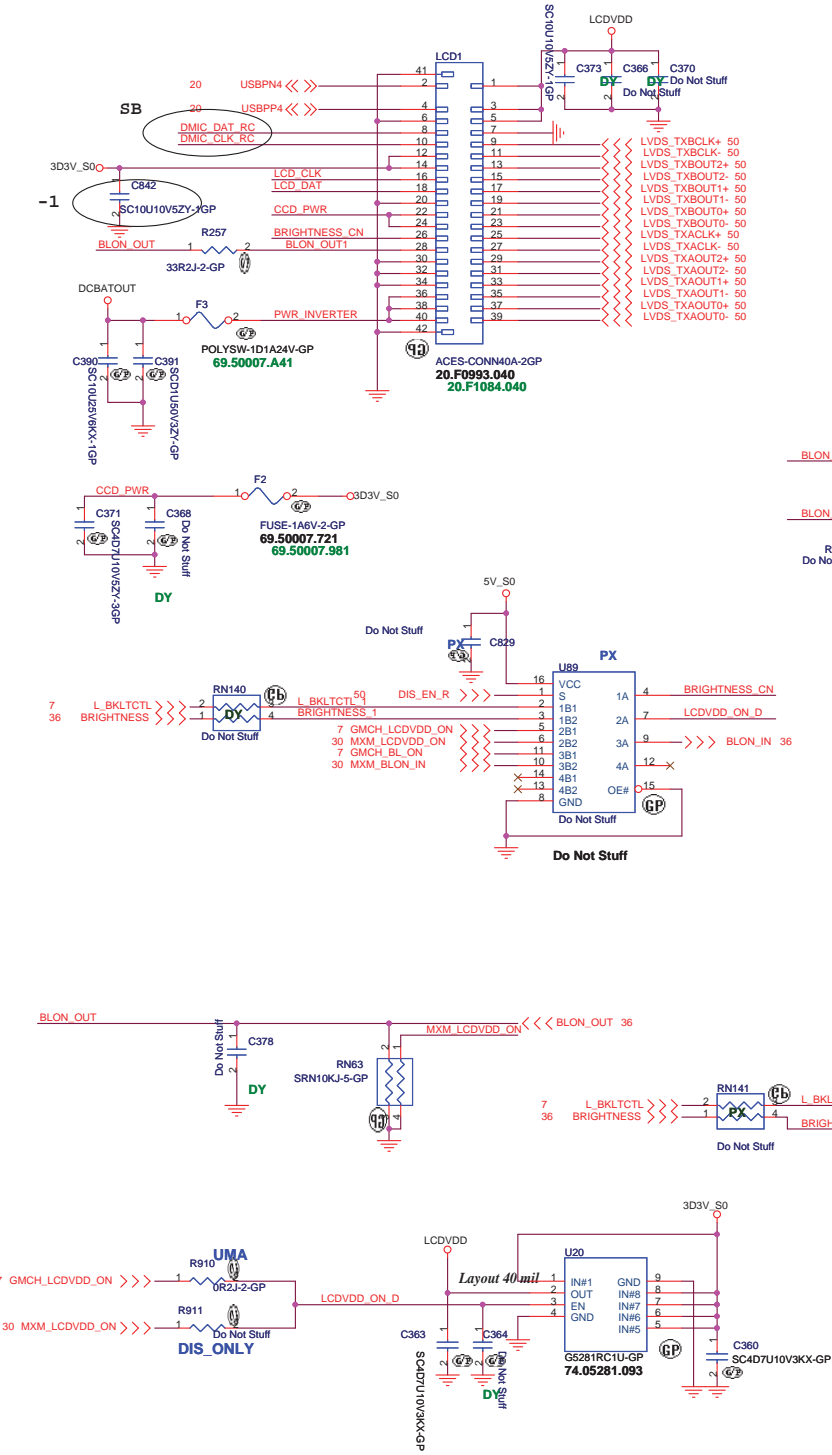


SJM80 UMA ONLY SB

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Taipei Hsien 221, Taiwan, R.O.C.

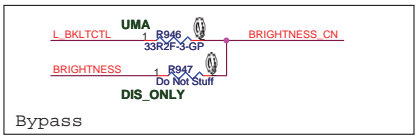
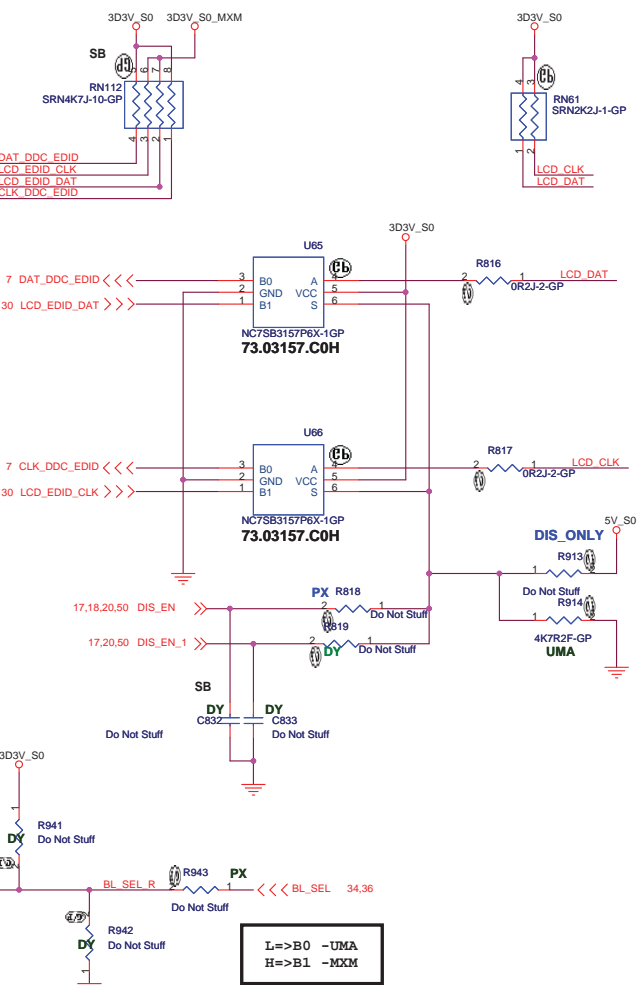
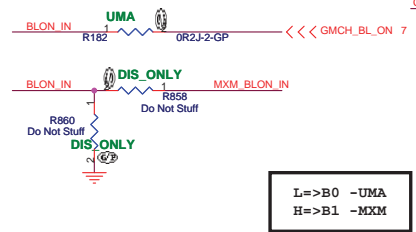
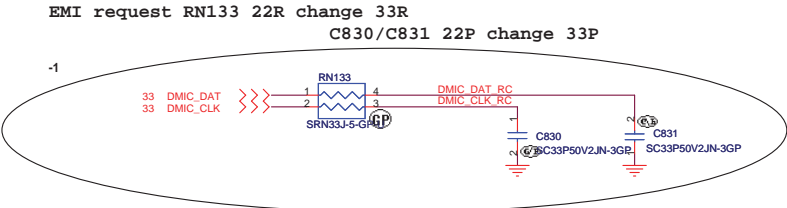
Title			
LAUNCH			
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LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



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Taipei Hsien 221, Taiwan, R.O.C.

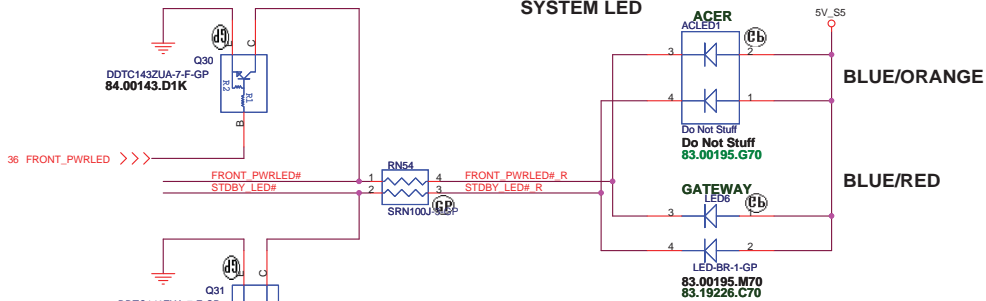
Title
LCD CONN

Size Document Number
SJM80/JV80

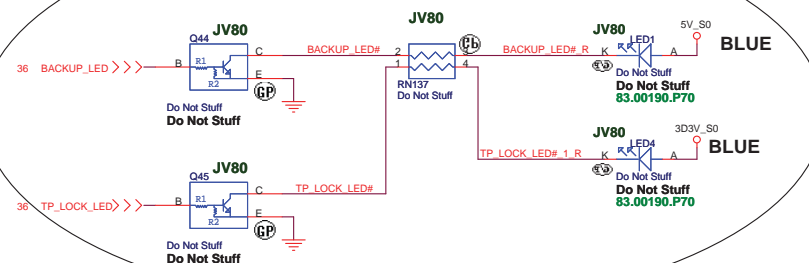
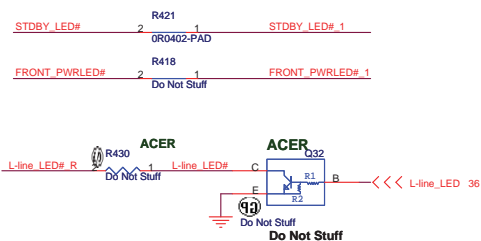
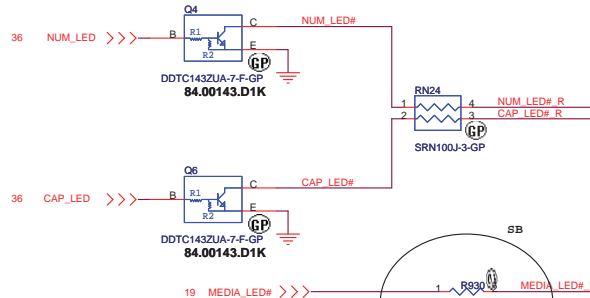
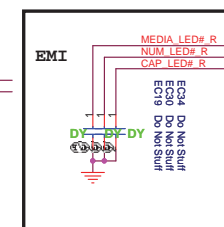
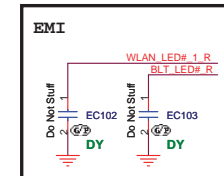
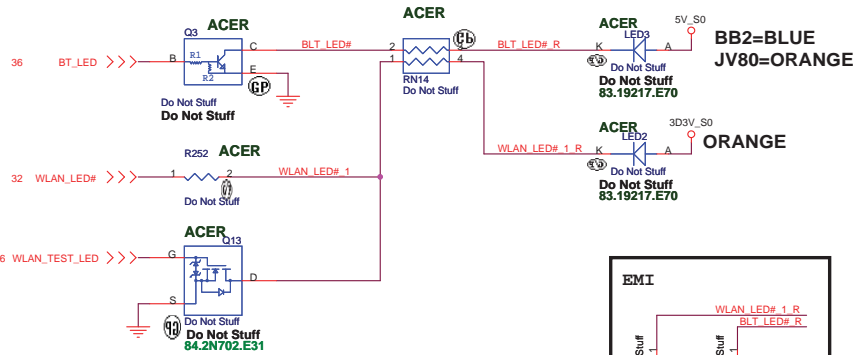
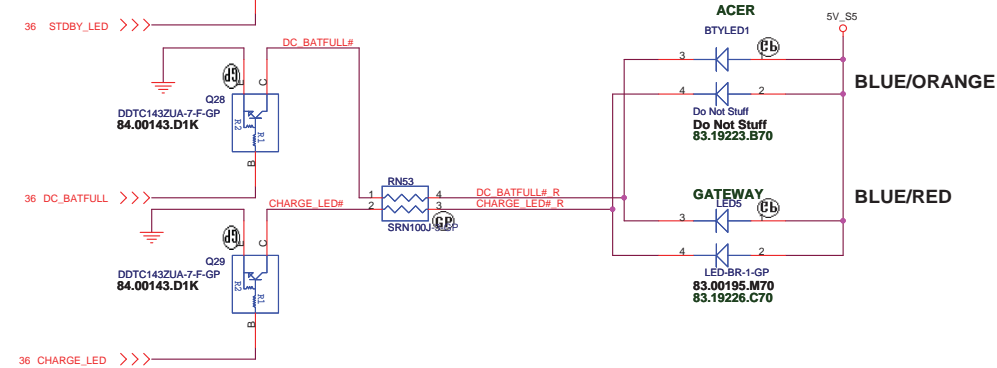
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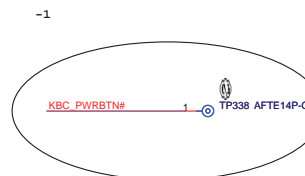
SYSTEM LED



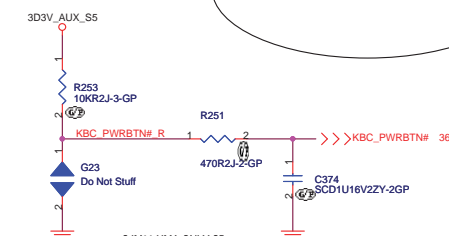
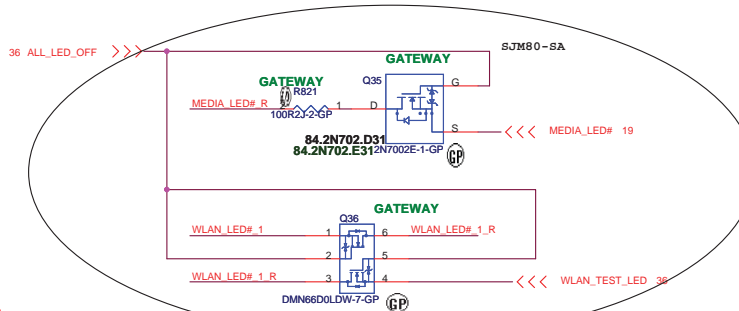
CHARGER LED



AFTE



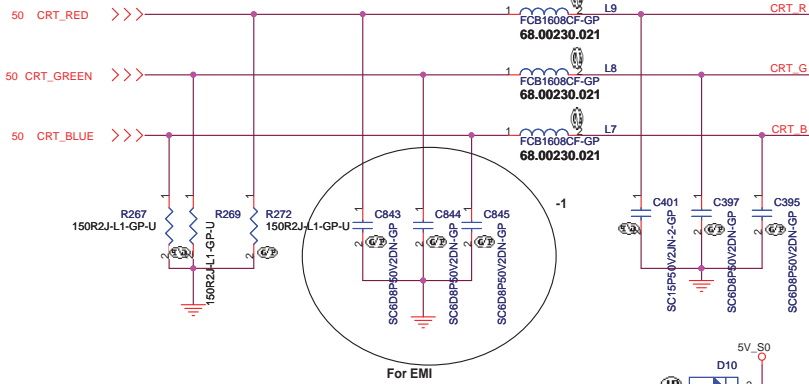
ALL LED OFF FUNCTION For GATEWAY



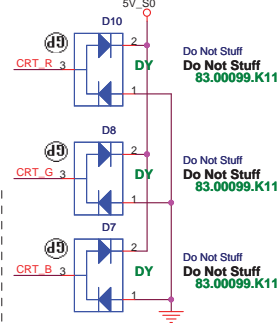
SJM80 UMA ONLY SB	
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Power & LED Board	
Size	Document Number
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2nd =68.00119.081 source Check

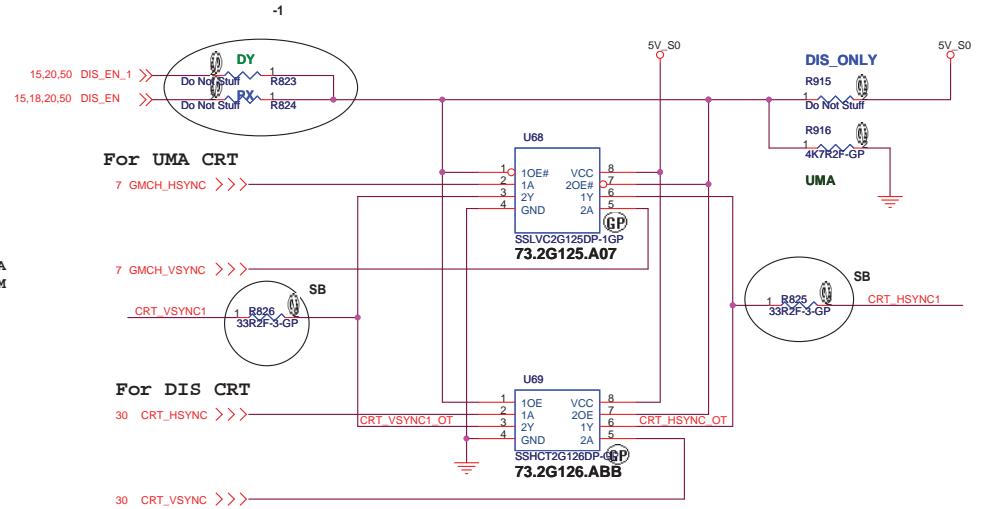
Ferrite bead impedance: 10 ohm@100MHz



Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



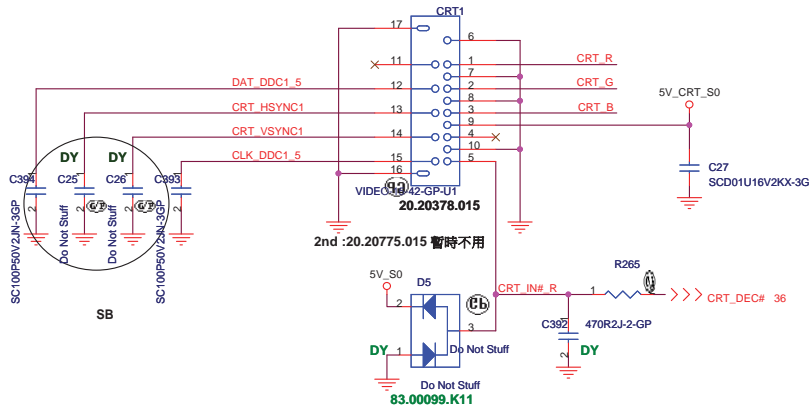
Hsync & Vsync level shift



For UMA CRT

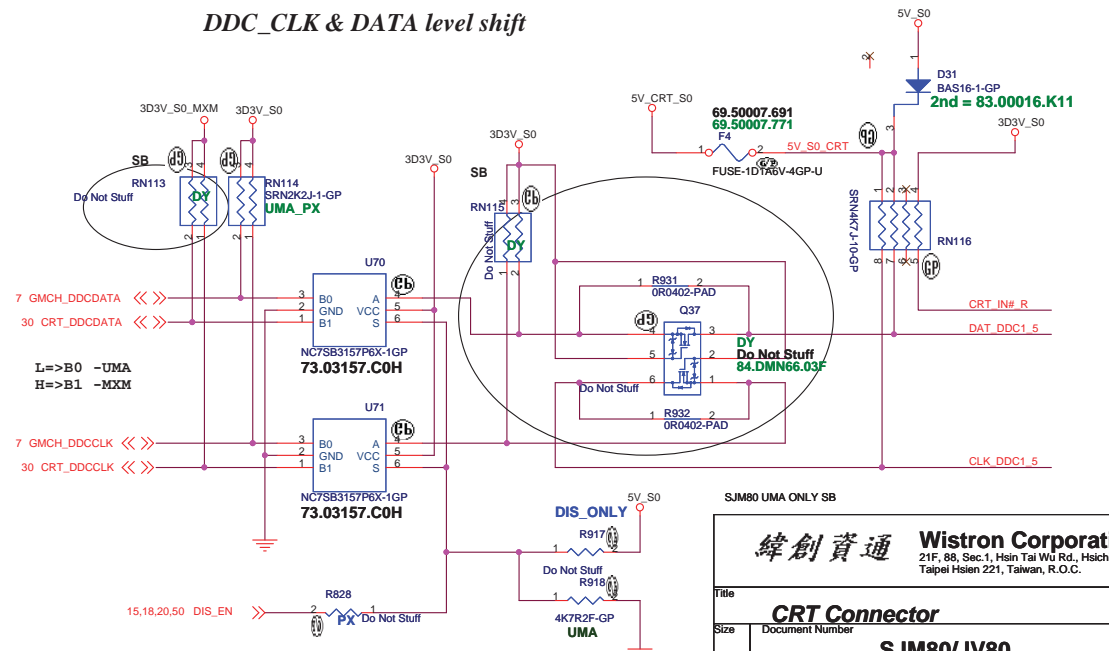
For DIS CRT

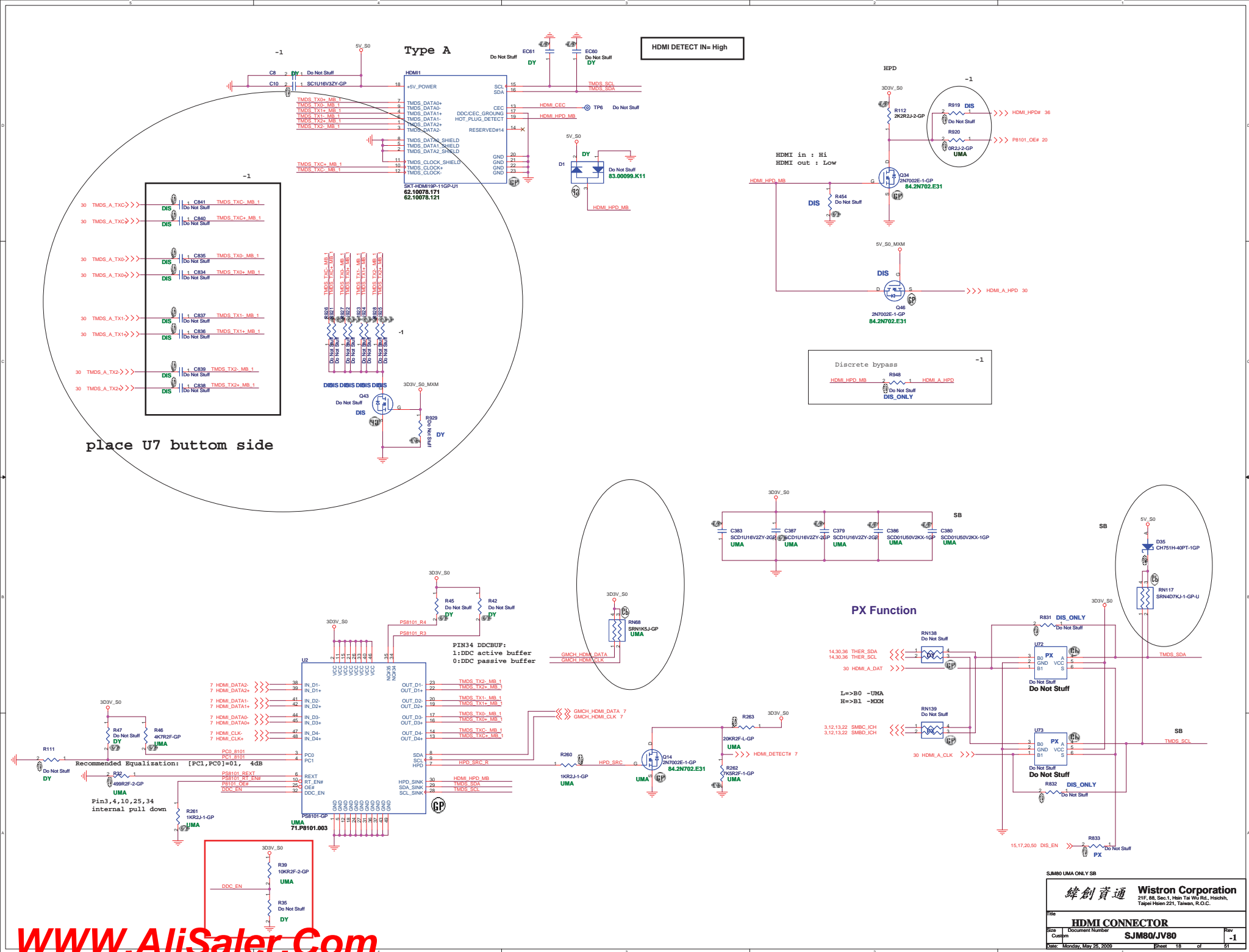
CRT I/F & CONNECTOR



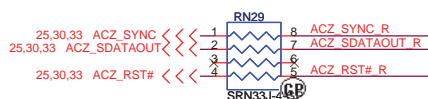
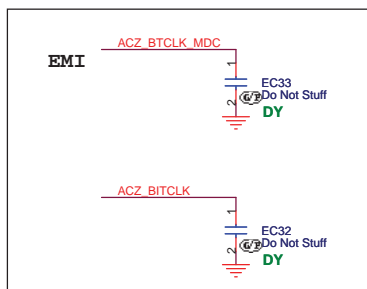
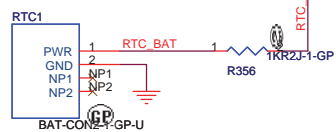
DDC_CLK & DATA level shift

DDC_CLK & DATA level shift

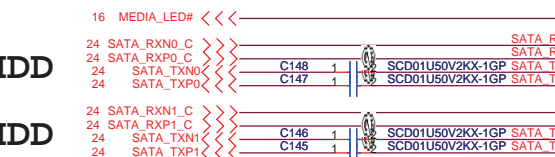
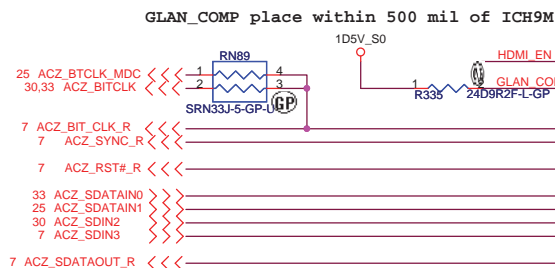
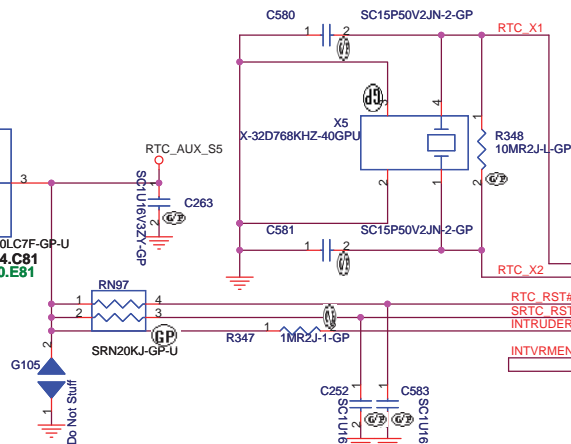
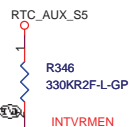




62.70001.011



PH=HDMI
PL=NO HDMI

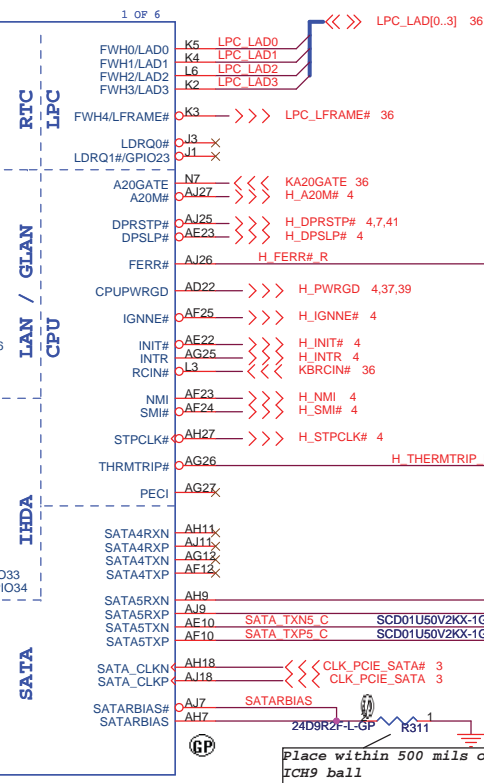


GLAN_COMP place within 500 mil of ICH9M

ICH9M-GP-NF
71.ICH9M.00U

71.ICH9M.C1U

integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable



Place within 500 mils of
ICH9 ball

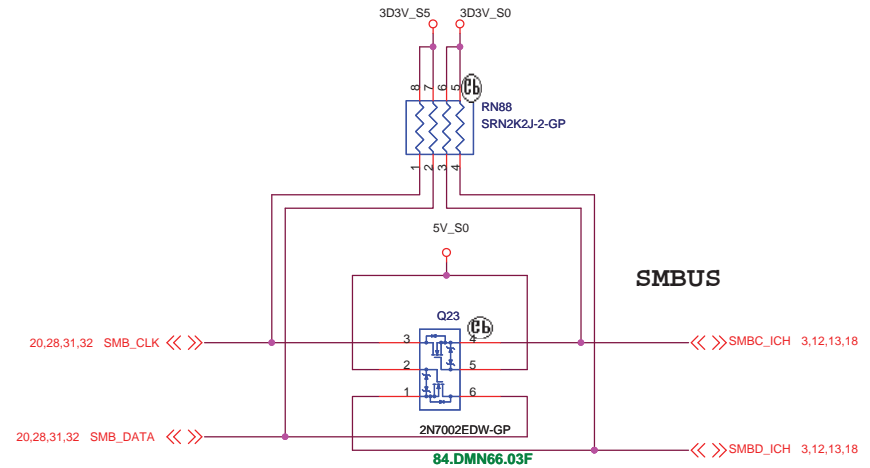
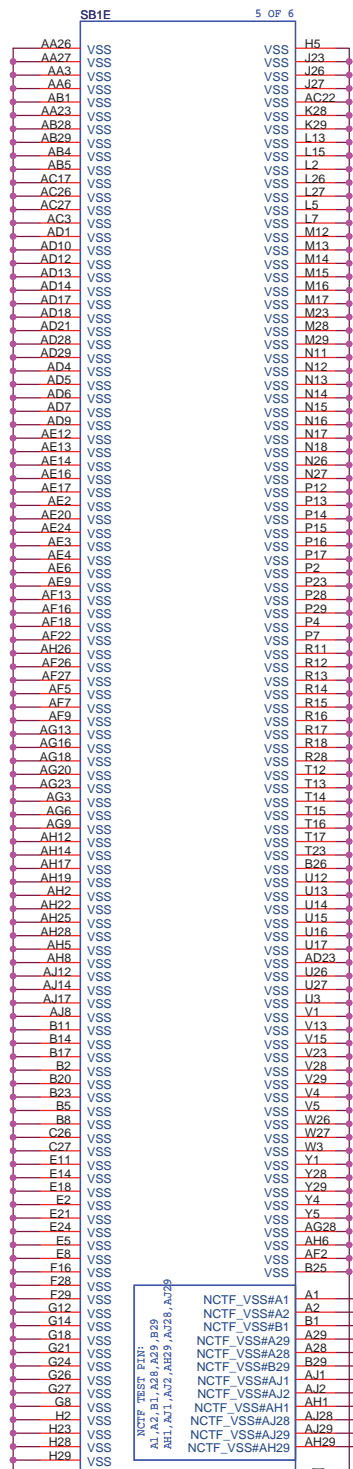
ODD

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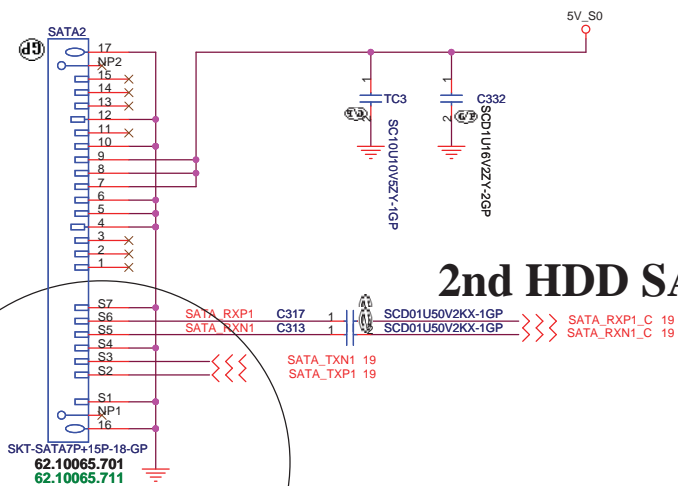
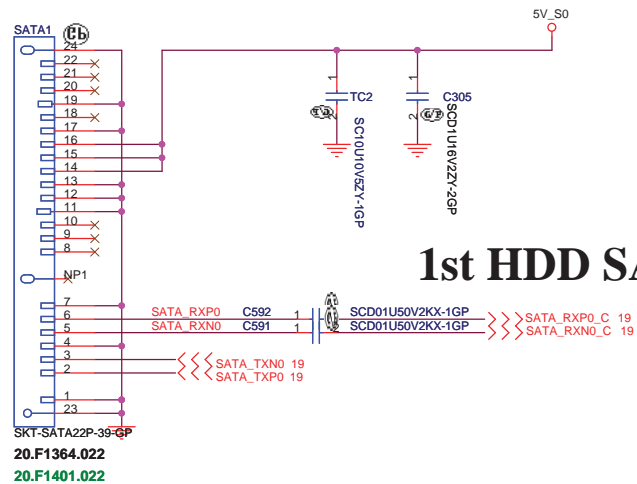
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title		ICH9-M (1 of 4)	
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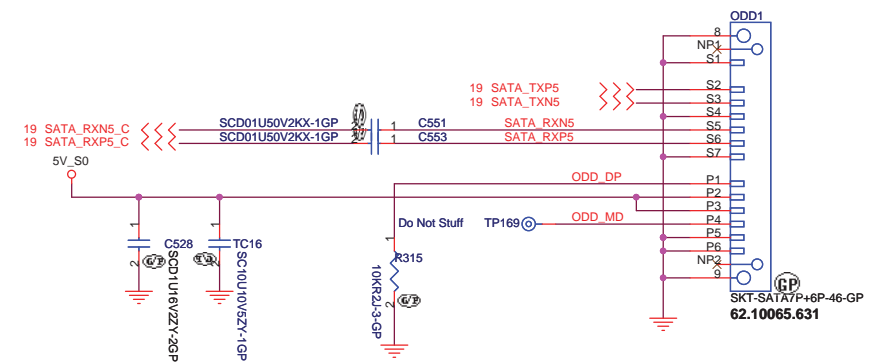






SB 不打Main source

SATA ODD Connector



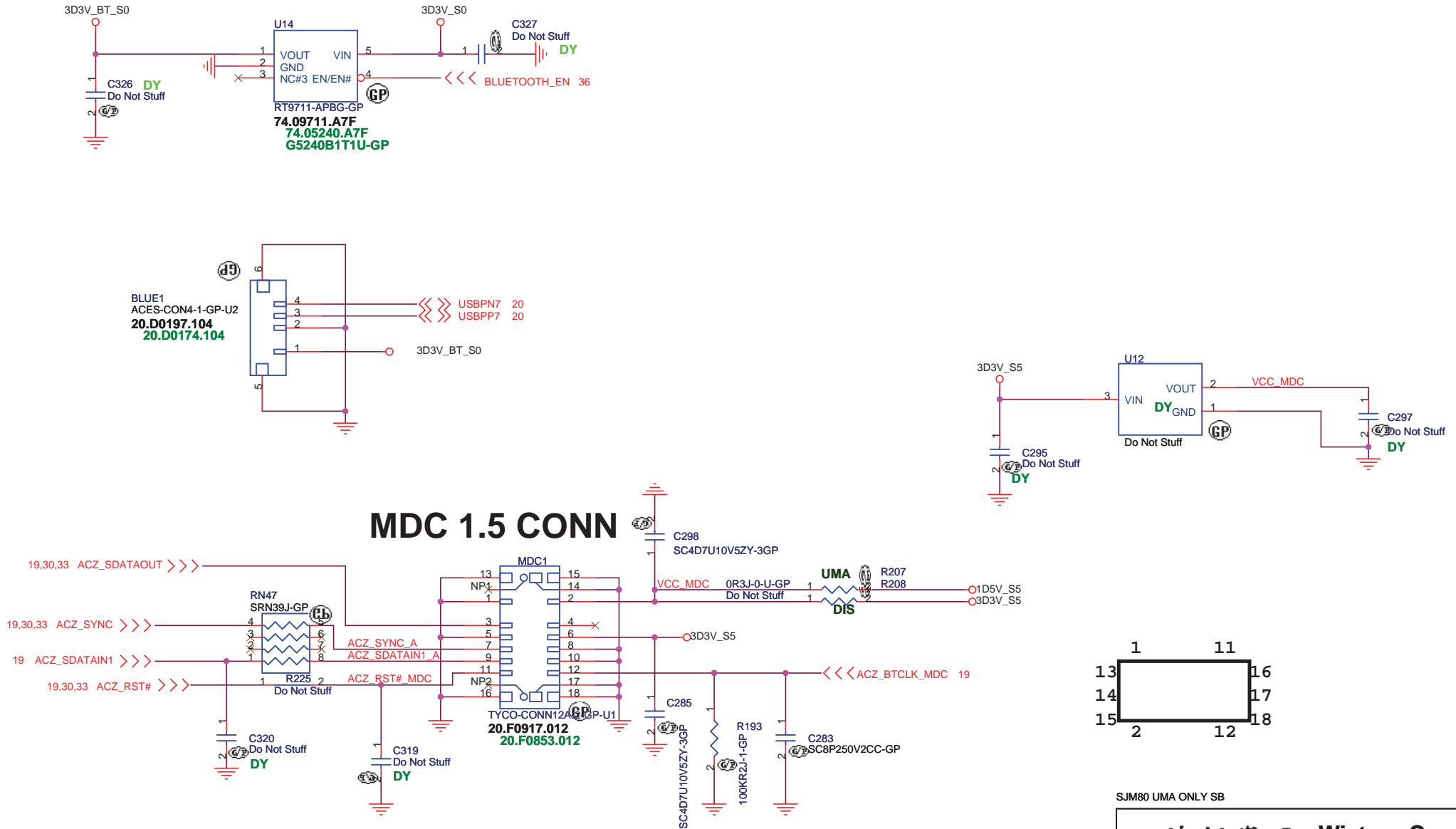
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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BLUETOOTH MODULE

1.5A / High Active Voltage 2V

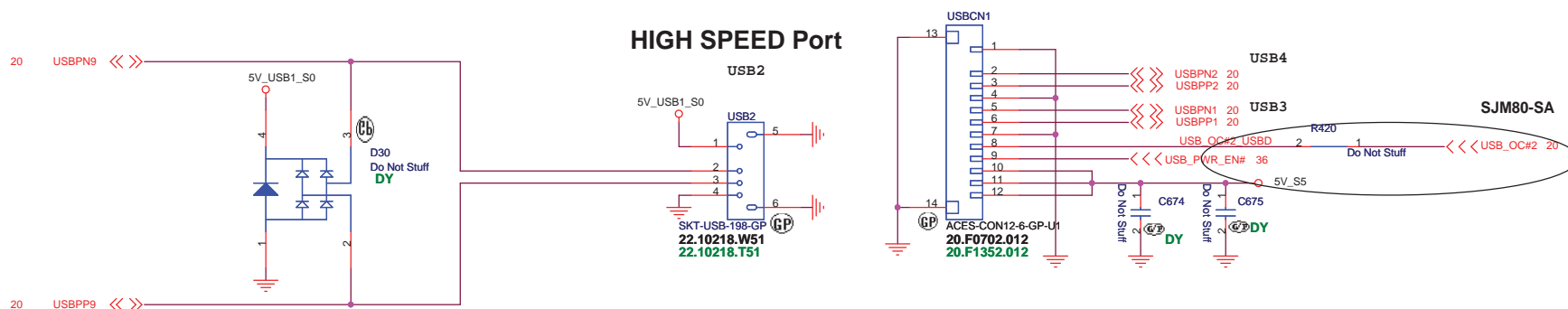
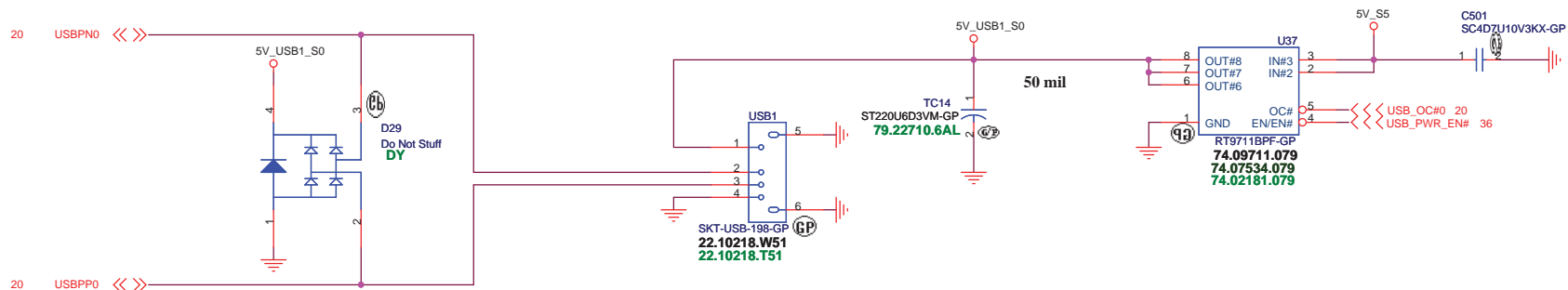


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緯創資通

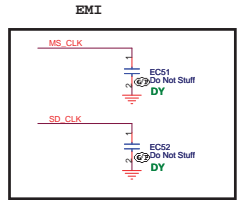
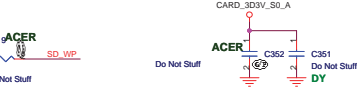
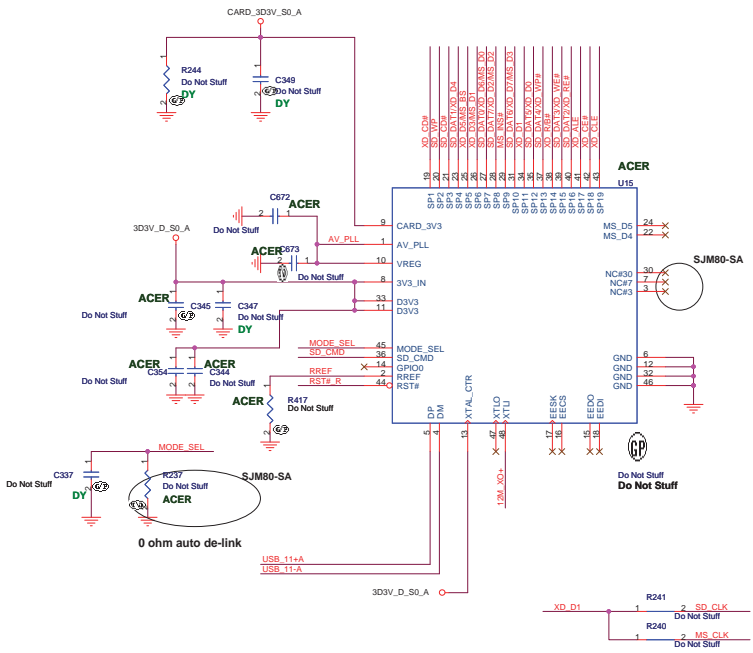
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)

CARD_3D3V_S0_A

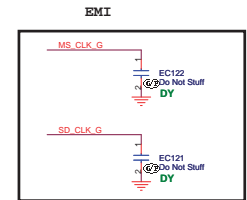
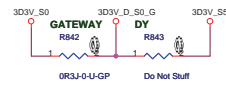
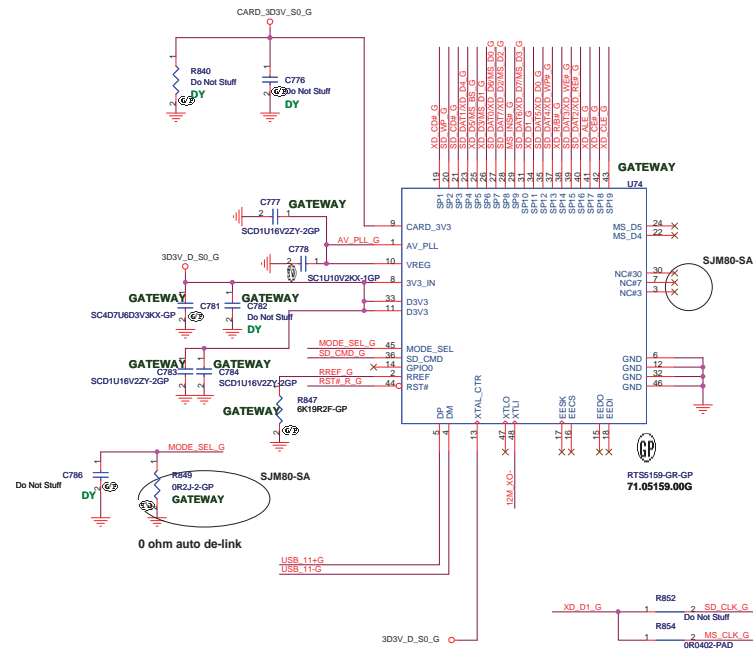
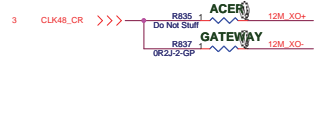
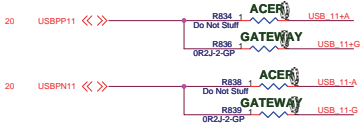
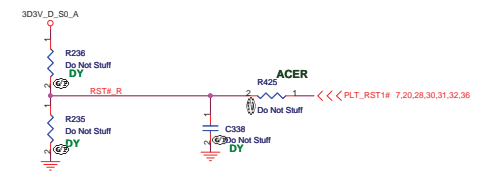
ACER

CARD1


	4	SD-VCC	XD-DAT0	22	SD_DAT5XD_D0
	19	SD-VCC	XD-DAT1	21	XD_D1
	29	MS-VCC	XD-DAT2	17	SD_DAT7XD_D2MS_D2
	28	MMC-DAT4	XD-DAT3	12	XD_D3MS_D1
SD_DAT4XD_WP#	28	MMC-DAT5	XD-DAT5	11	SD_DAT1XD_D4
SD_DAT5XD_D0	24	MMC-DAT6	XD-DAT6	8	XD_D5MS_D5
SD_DAT6XD_D7MS_D3	24	MMC-DAT7	XD-DAT7	7	SD_DAT0XD_D6MS_D0
SD_DAT6XD_D2MS_D0	13			6	SD_DAT6XD_D7MS_D3
SD_D6MS_BS	14	MS-BS	XD-32	32	SD_DAT4XD_WP#
MS_INS#	23	MS-INS	XD-33	33	SD_DAT7XD_D2MS_D2
MS_SCLK	27	MS-SCLK	XD-34	34	XD_ALE
SD_DAT0XD_D6MS_D0	18	MS-DAT0	XD-CLE	36	XD_CLE
SD_DAT1XD_D4	16	MS-DAT1	XD-37	38	XD_CE#
SD_DAT7XD_D2MS_D0	22	MS-DAT2	XD-38	37	SD_DAT2XD_RE#
SD_DAT6XD_D7MS_D3	25	MS-DAT3	XD-R#	38	XD_R#
		SD-CD#	XD_CD	40	XD_CD#
SD_CD#	1	SD_CD#			
SD_WP#	2	SD_WP	NP1		NP1
SD_CLK#	15	SD_CLK	NP2		NP2
SD_CMD	16	SD_CMD			
SD_DAT0XD_D6MS_D0	8	SD-DAT0	79N_D0	3	
SD_DAT1XD_D4	5	SD-DAT1	79N_D1	39	
SD_DAT2XD_RE#	31	SD-DAT2	79N_D2	41	
SD_DAT3XD_WE#	30	SD-DAT3	79N_D3	42	

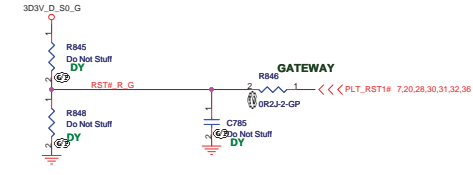
Do Not Solder

Do Not Solder



CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)

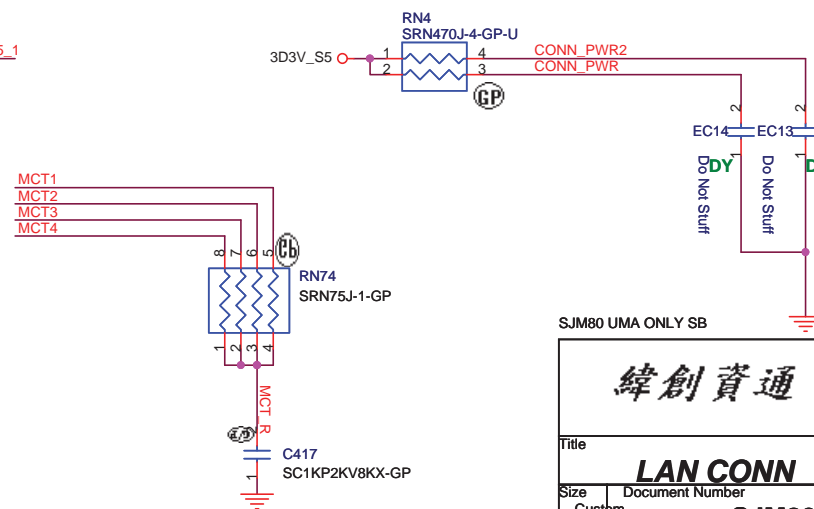
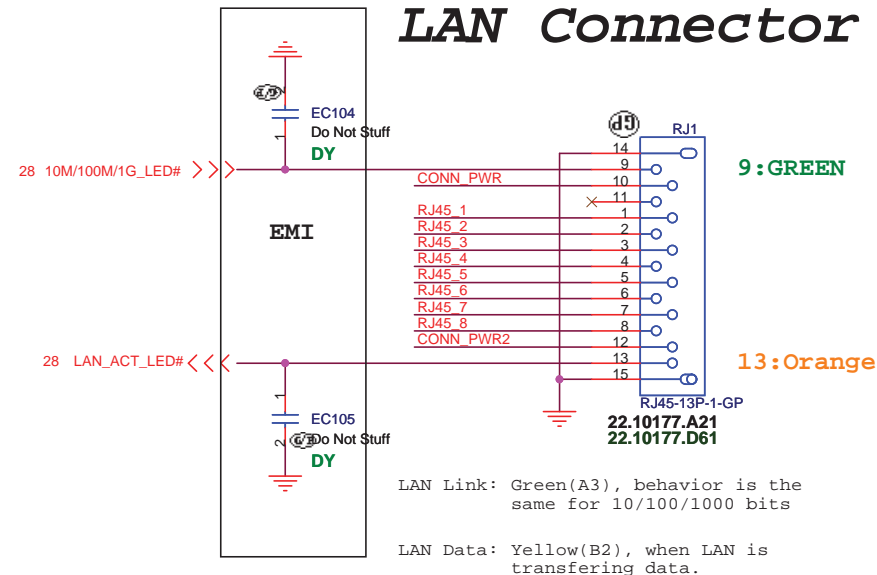
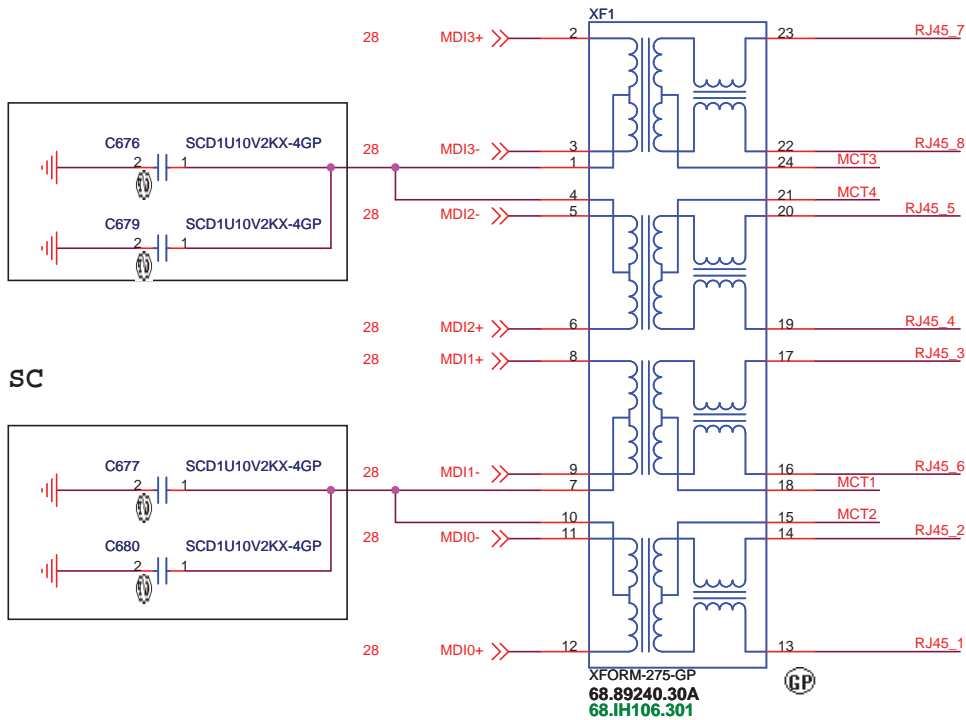
CARD3D_V0_S0_G		CARD2		GATEWAY		
		23	SD_VCC	SD_DAT0	25	SD_D0
		14	MS_VCC	SD_DAT1	26	SD_D1
		33	XD_VCC	SD_DAT2	10	SD_D2
				SD_DAT3	11	SD_D3
SD_DAT5XD_D0_G	8	XD_D0	SD_CMD	12	SD_D4	
SD_D1_G	14	XD_D1	SD_CLK	24	SD_D5	
SD_DAT4XD_D2MS_D2_G	26	XD_D2	SD_CD#	36	SD_D6	
XD_D3MS_D1_G	27	XD_D3	SD_WP#_SD	38	SD_D7	
XD_D5MS_SS_G	30	XD_D4				
SD_DAT3XD_RE_G	31	XD_D5				
SD_DAT5XD_D3_G	32	XD_D6	MS_DAT0A	18	SD_D0	
		XD_D7	MS_DAT1A	20	SD_D1	
XD_R#G	1	XD_R#	MS_DAT2A	18	SD_D2	
SD_DAT2XD_RE#_G	2	XD_RE	MS_DAT3A	18	SD_D3	
XD_CE#_G	3	XD_CE	MS_B1	21	XD_D0	
XD_CLE#_G	4	XD_CLE	MS_B2	17	MS_D0	
XD_ALE#_G	5	XD_ALE	MS_SCL#	15	MS_C0	
SD_DAT4XD_WE#_G	6	XD_WE				
SD_DAT6XD_WP#_G	7	XD_WP				
XD_CD#_G	34	XD_CD_SW	4N1_GND	13	22	
			4N1_GND	38	38	
			4N1_GND	38	38	
			4N1_GND	38	38	
</						





LAN Connector

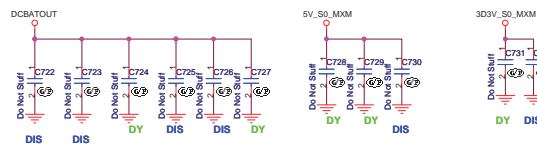
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



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PX Function

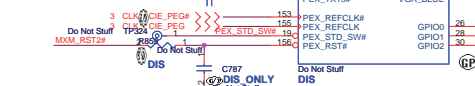
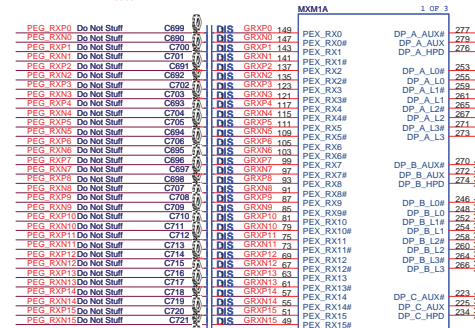


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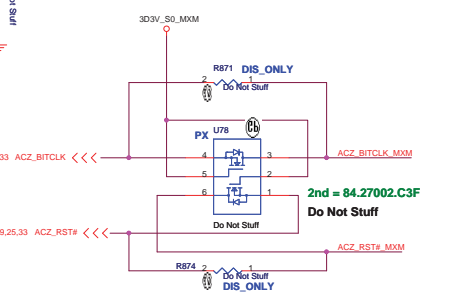
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7 PEG_TXN[15..0] << >>

7 PEG_RXP[15..0] << >>
7 PEG_RXN[15..0] << >>

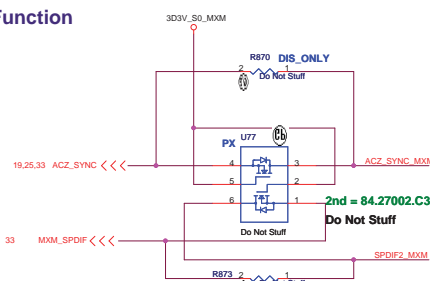
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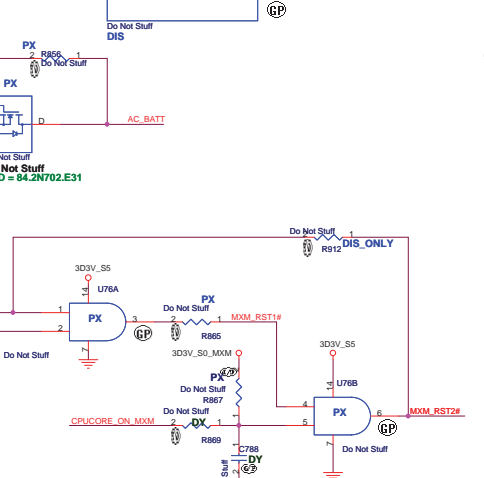
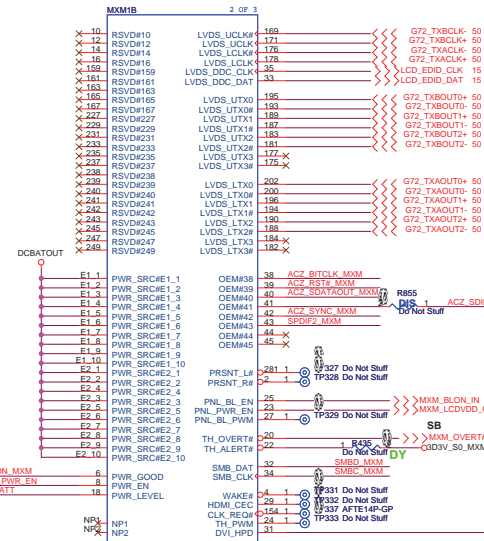
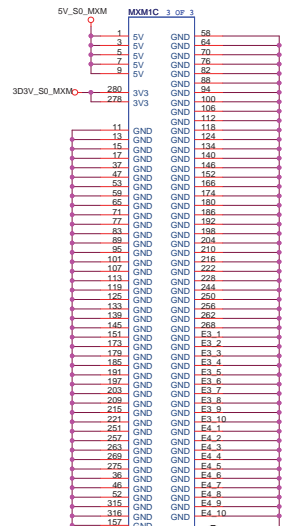
PX Function



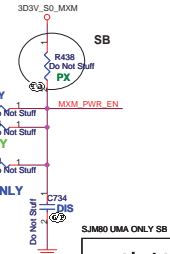
PX Function



PX Function

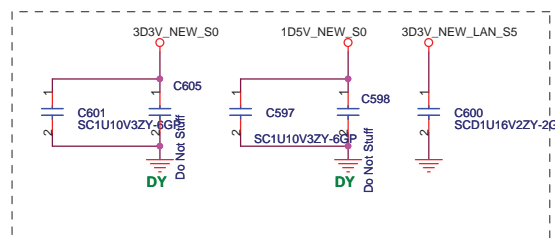
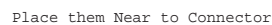
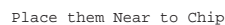


PX Function



Reserve the symbol
for bottom side
connector

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NEW CARD

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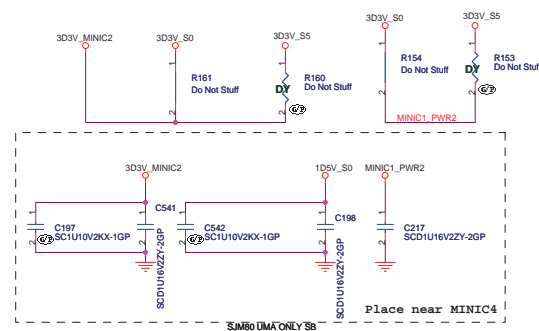
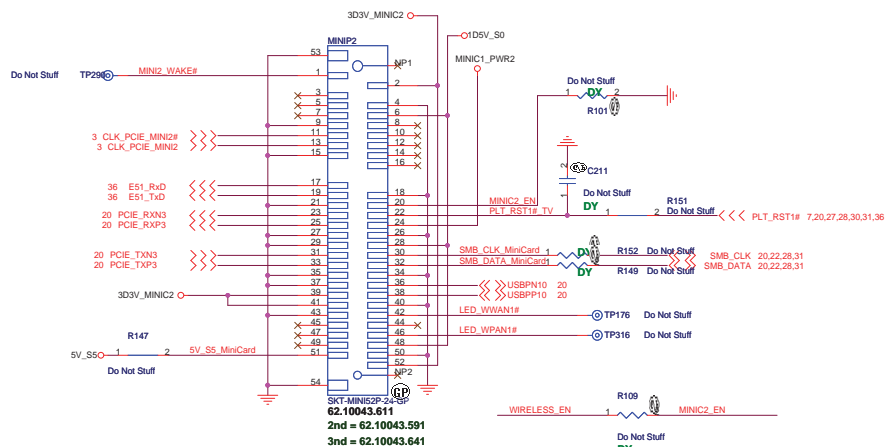
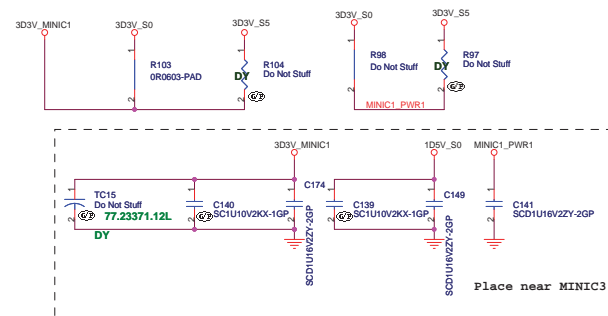
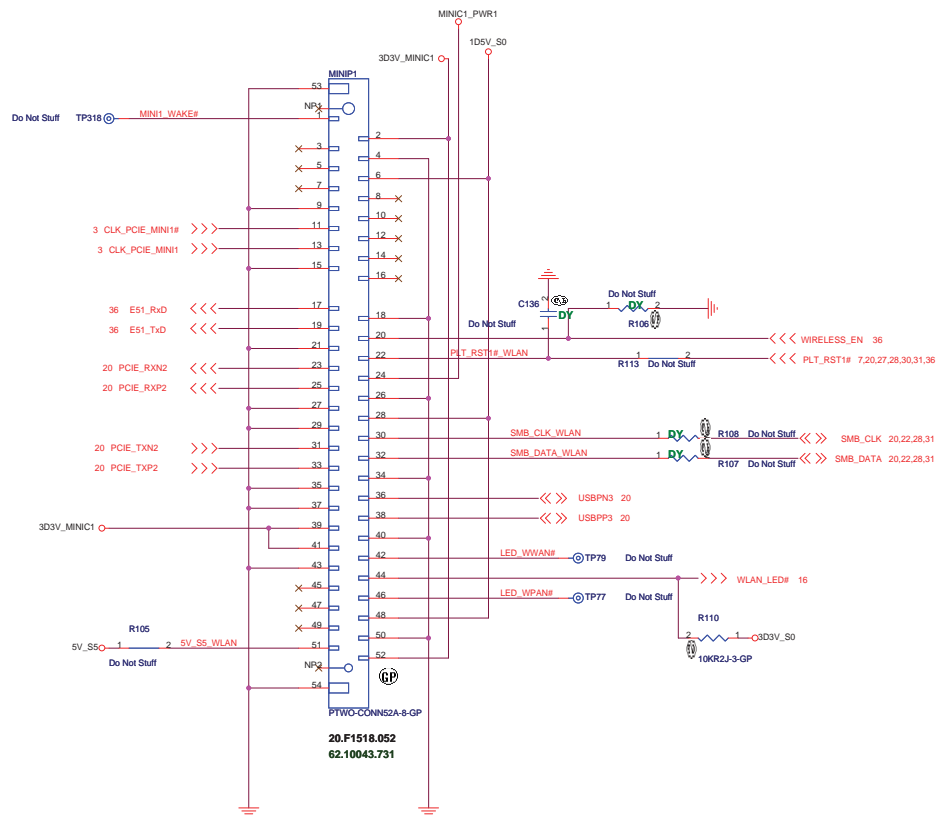
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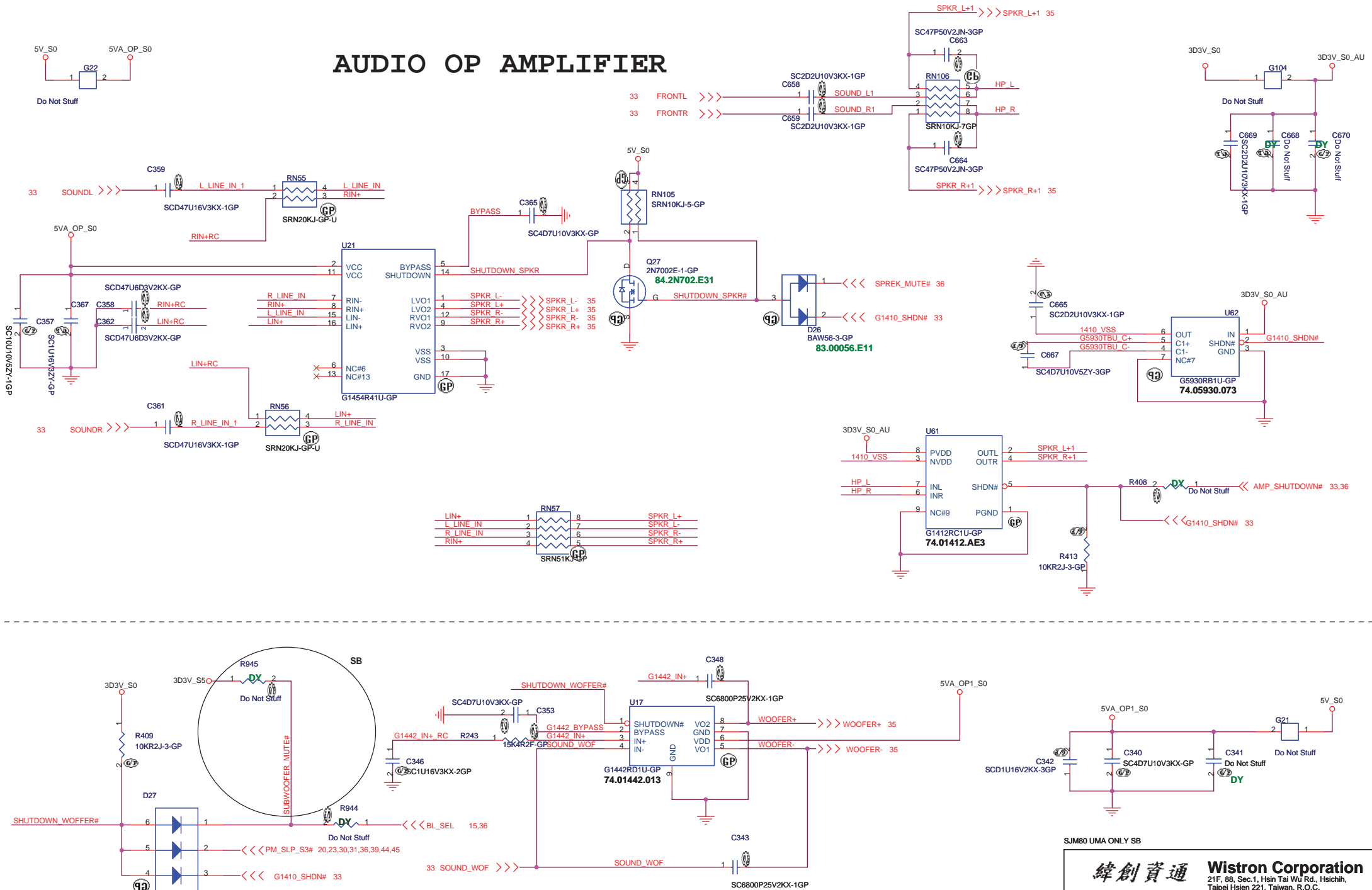
Mini Card Connector(WLAN)

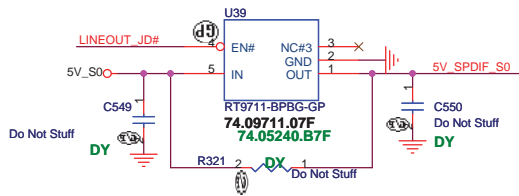


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MINI CARD			
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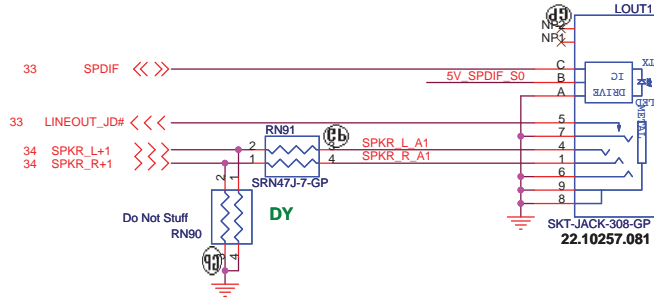
AUDIO OP AMPLIFIER



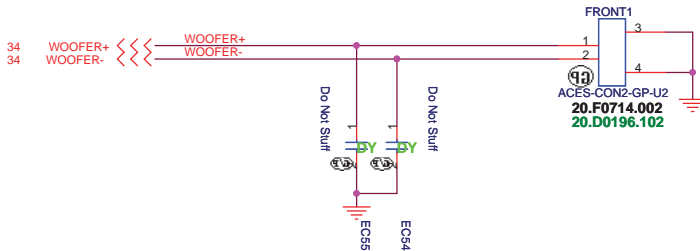


LINE OUT

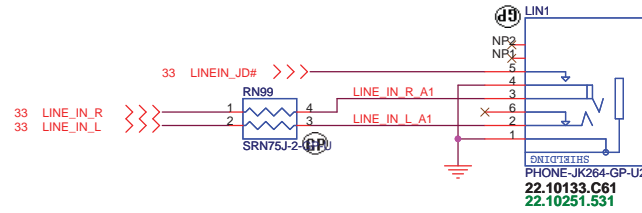
Delete 2nd source



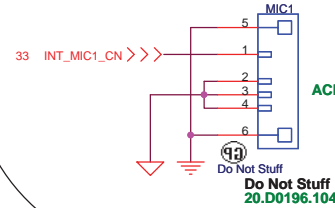
SUBWOOFER



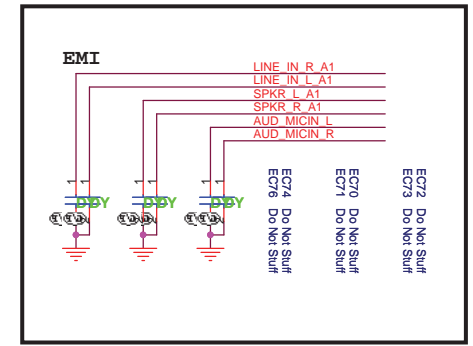
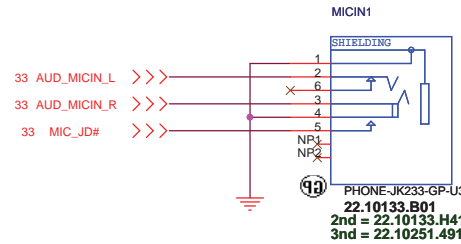
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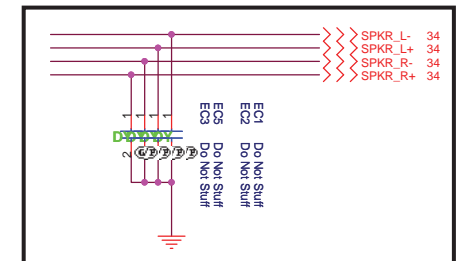
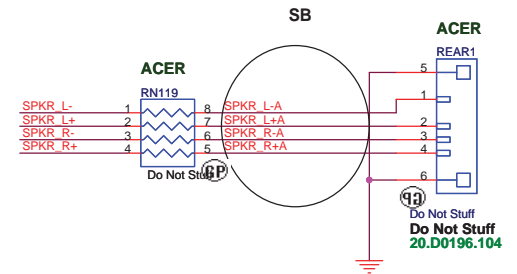
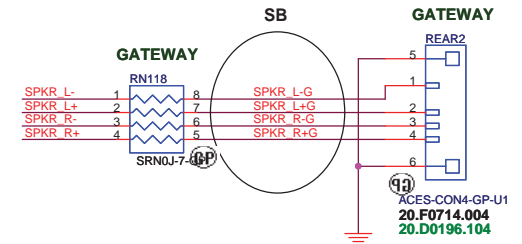
INT. MIC



MIC IN



REAR Speaker

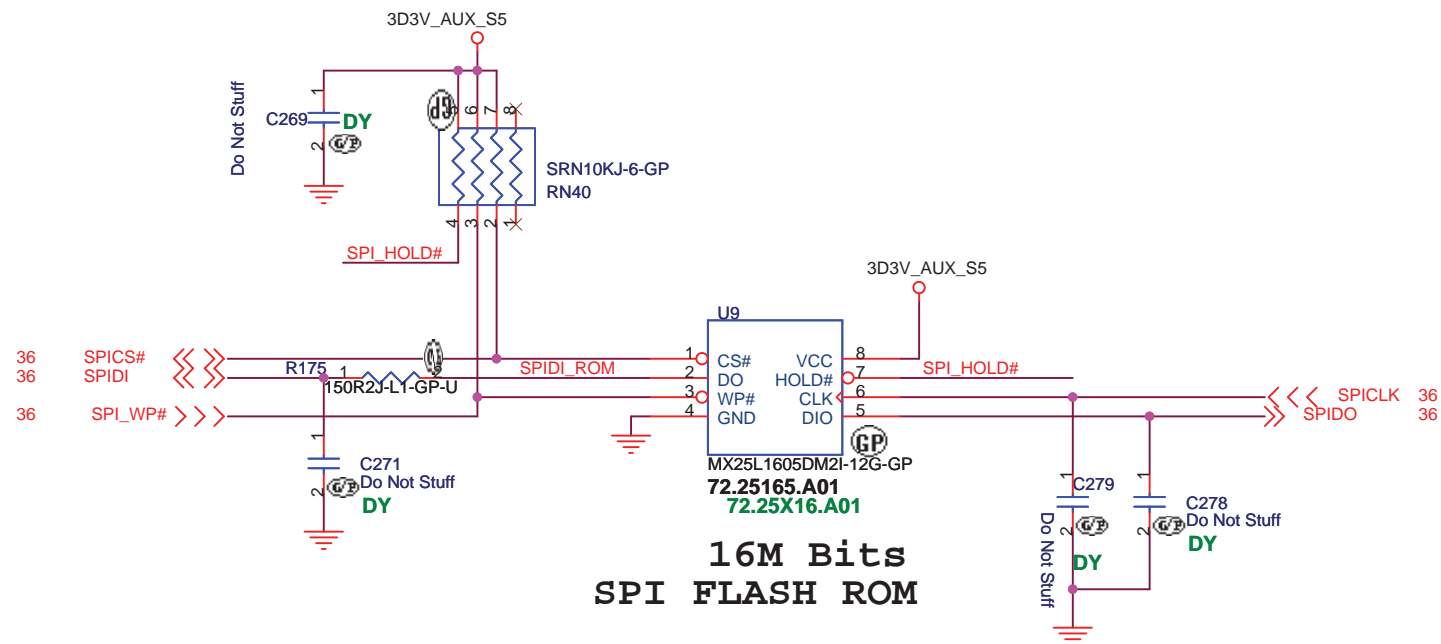


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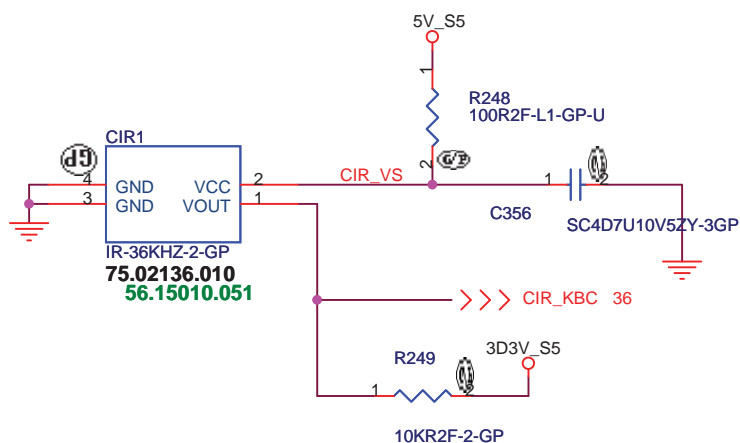
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CIR Module



Check test point

3D3V_S0	TP202 TPAD14-GP
3D3V_AUX_S5	TP141 Do Not Stuff
3D3V_S5	TP120 Do Not Stuff
5V_S5	TP130 Do Not Stuff
20,36 PM_PWRBTN#	TP115 Do Not Stuff
4,19,39 H_PWRGD	TP320 Do Not Stuff
36,39 S5_ENABLE	TP110 Do Not Stuff
4,6 H_CPURST#	TP278 Do Not Stuff

Test Point放在Dimm Door打開可量測處

SJM80 UMA ONLY SB

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

BIOS

Size

Document Number

Rev

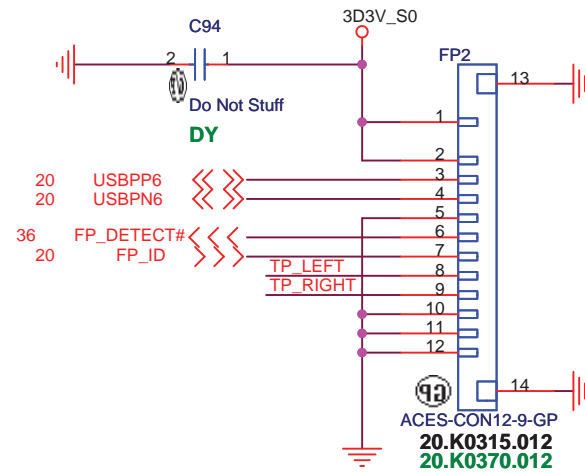
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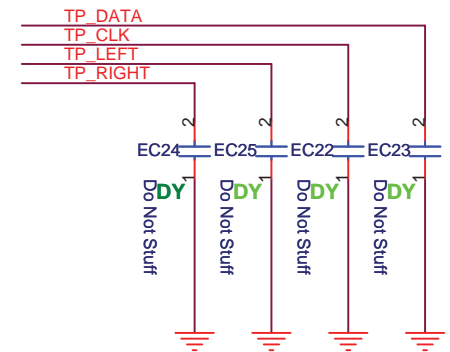
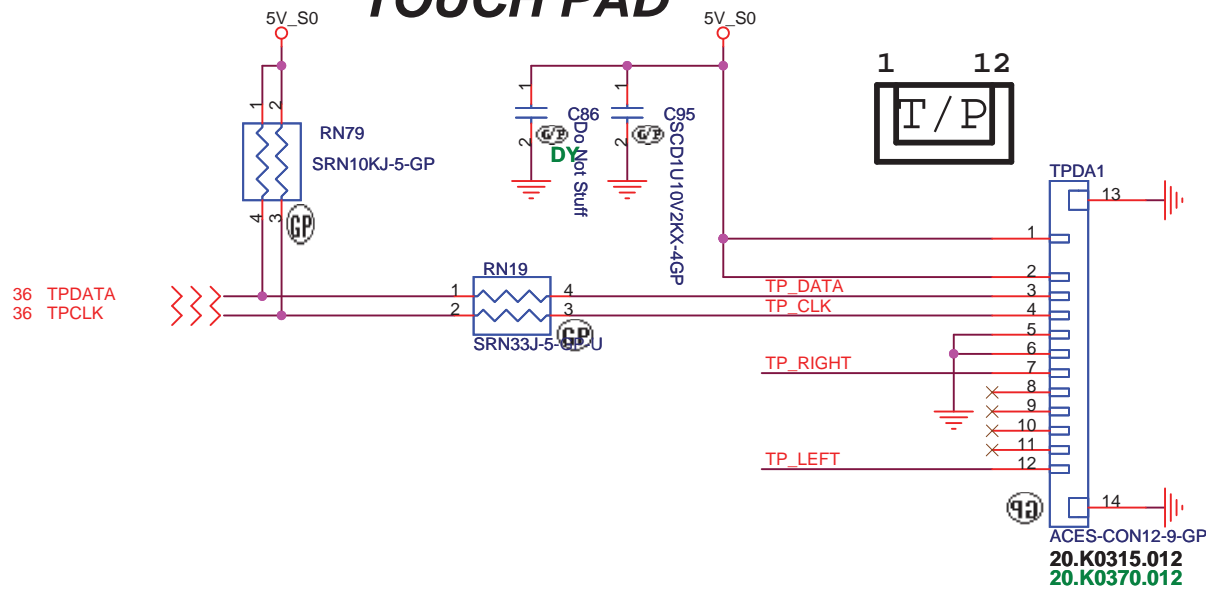
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Finger printer



TOUCH PAD

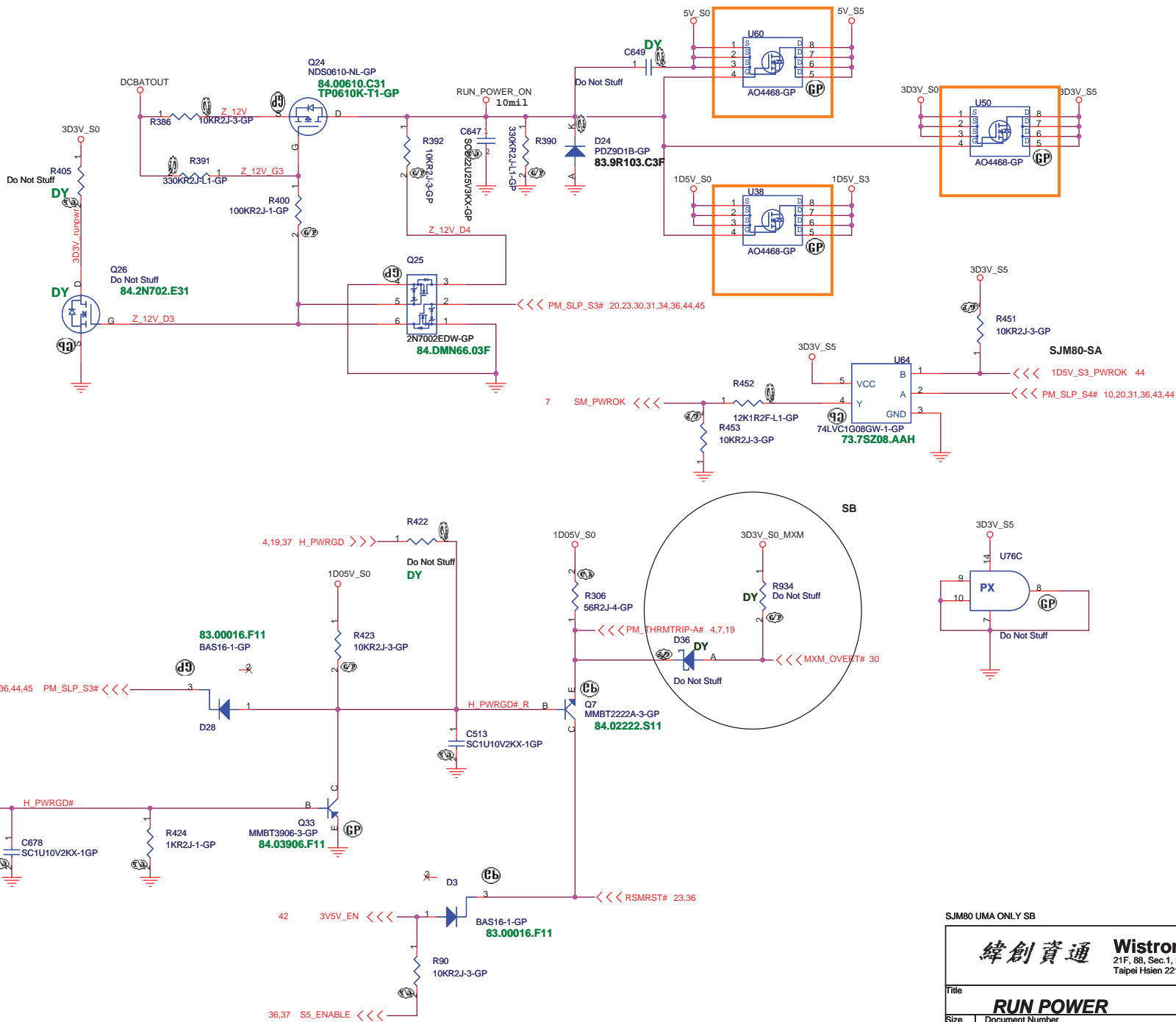


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Finger Printer and Touch PAD		
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Run Power



SJM80 UMA ONLY SE

緯創資通

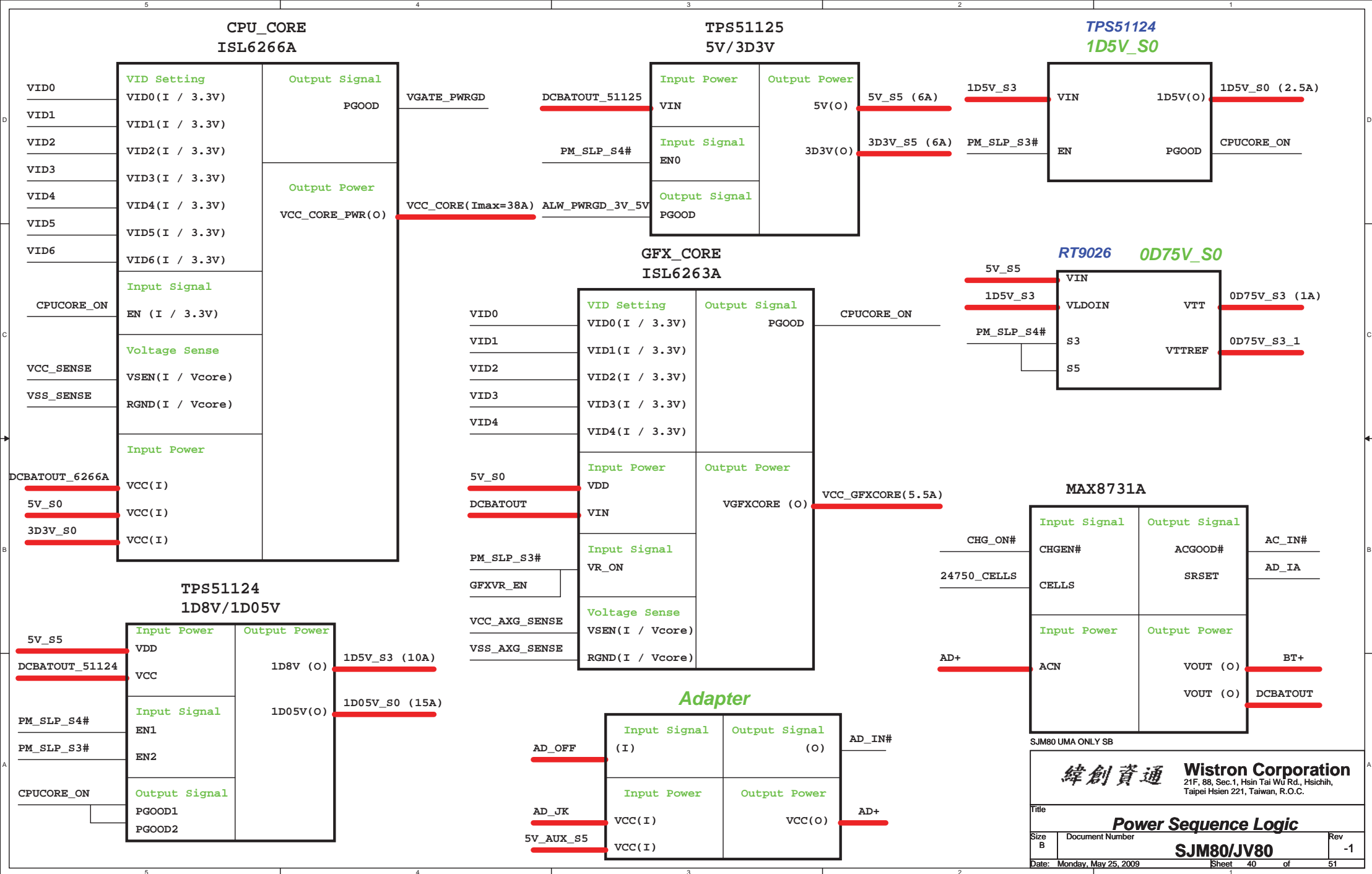
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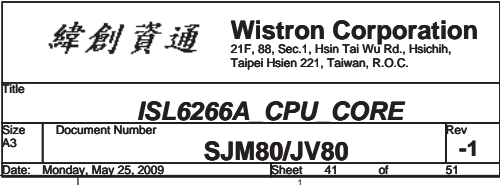
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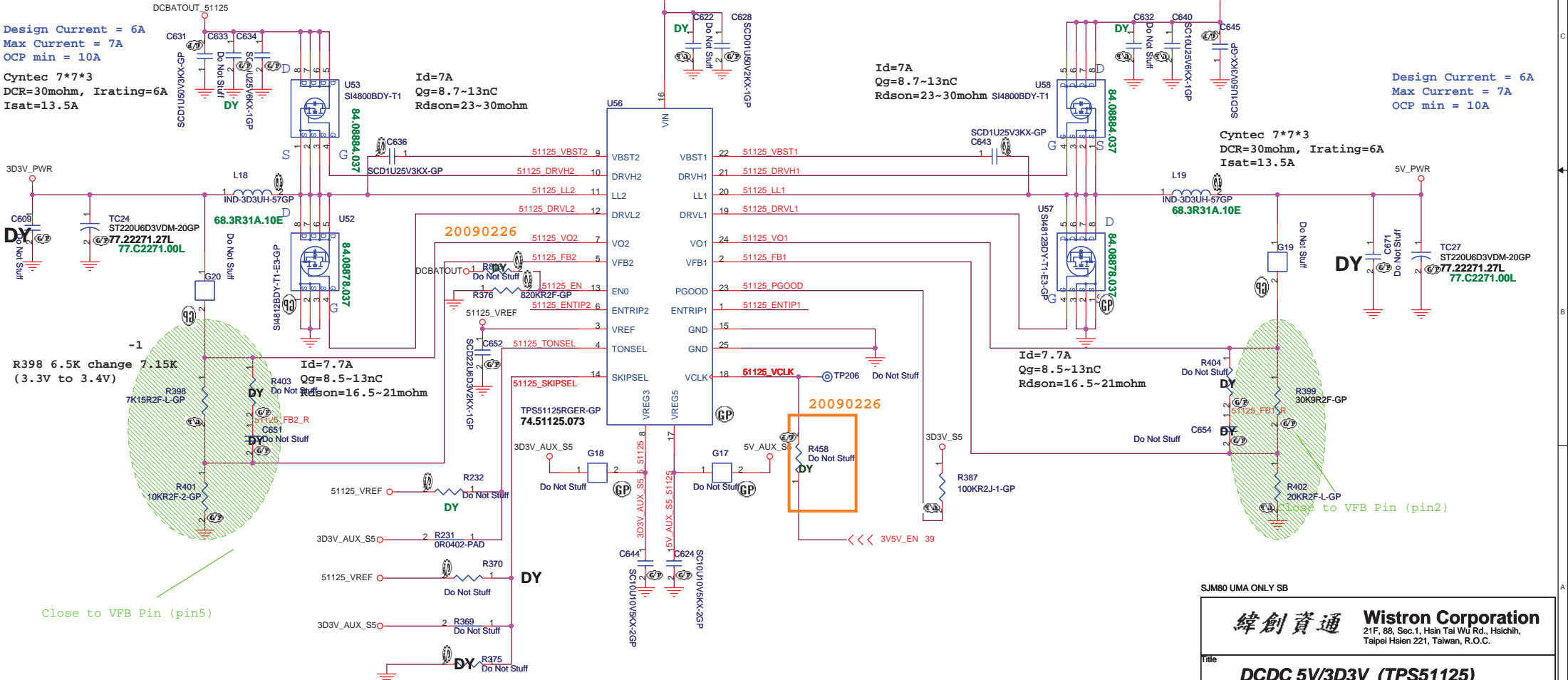
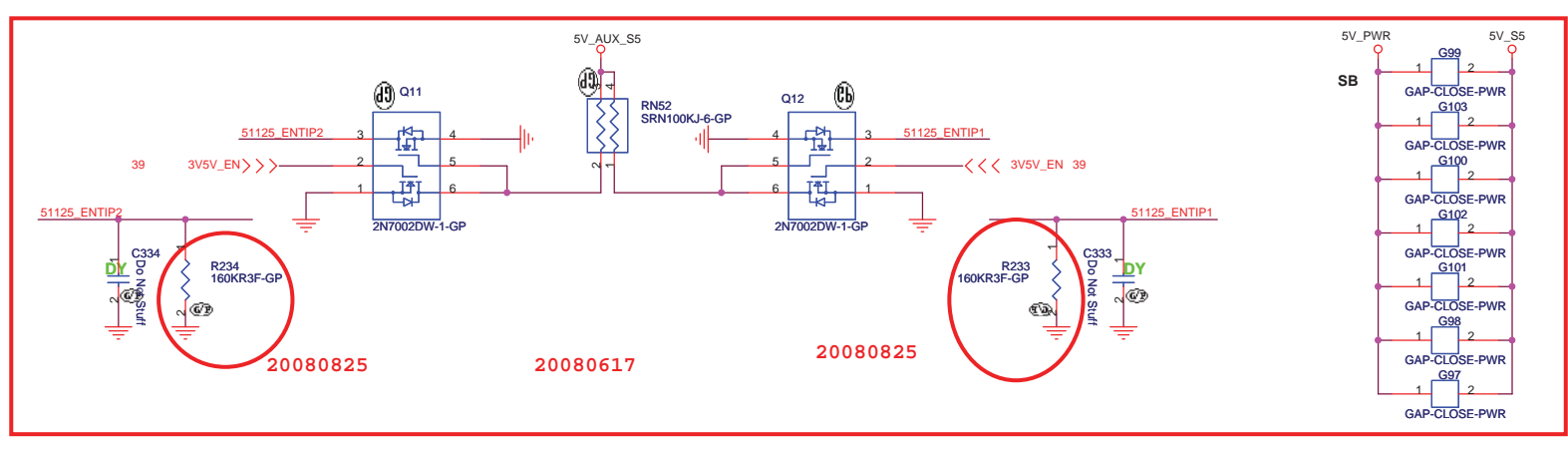
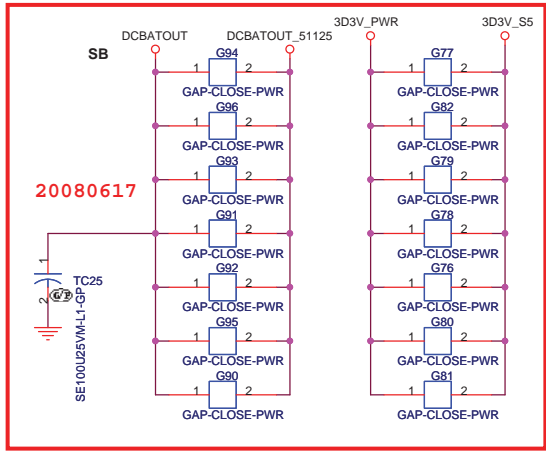
RUN POWER

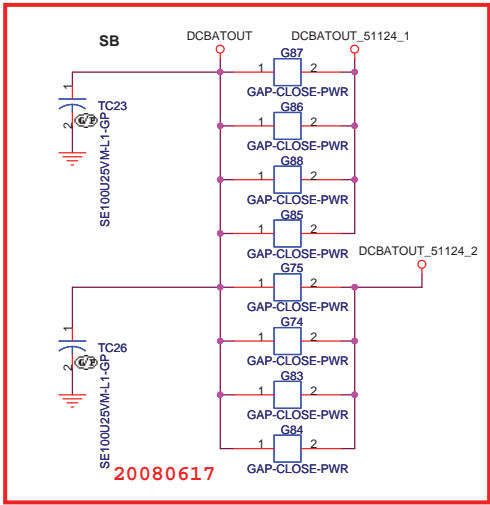
Size	Document Number
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SJM80/JV80





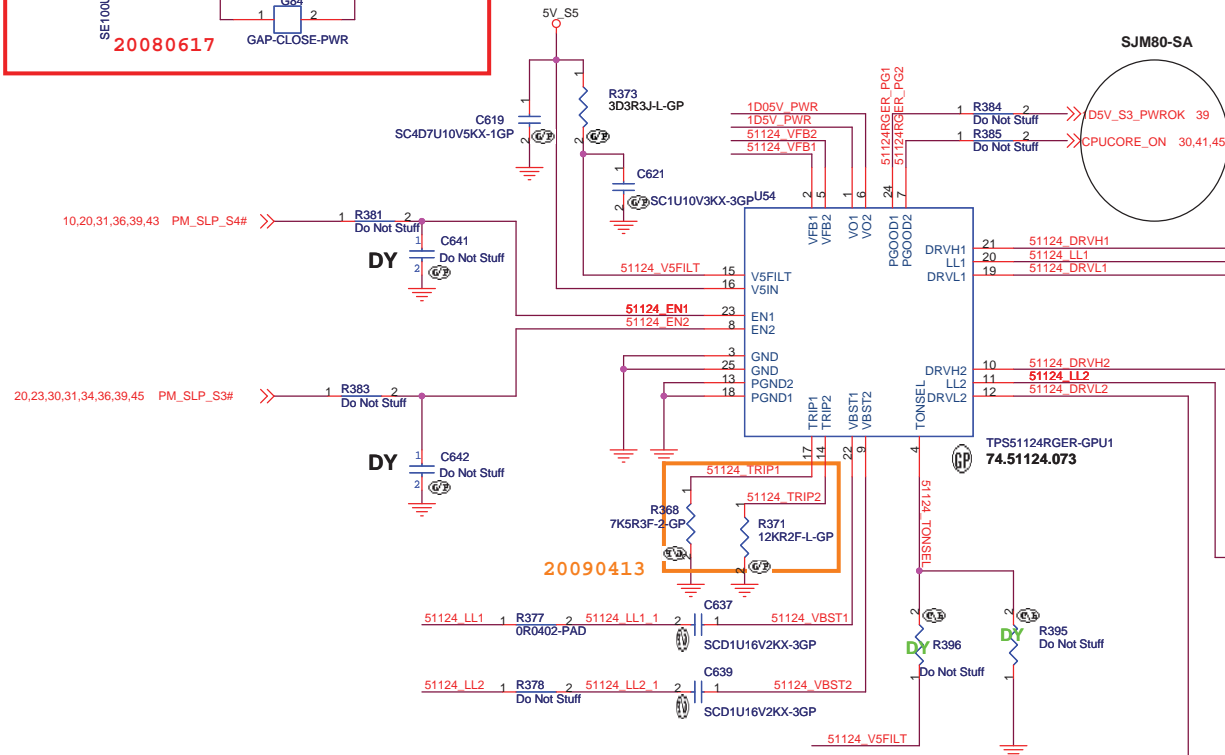




$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

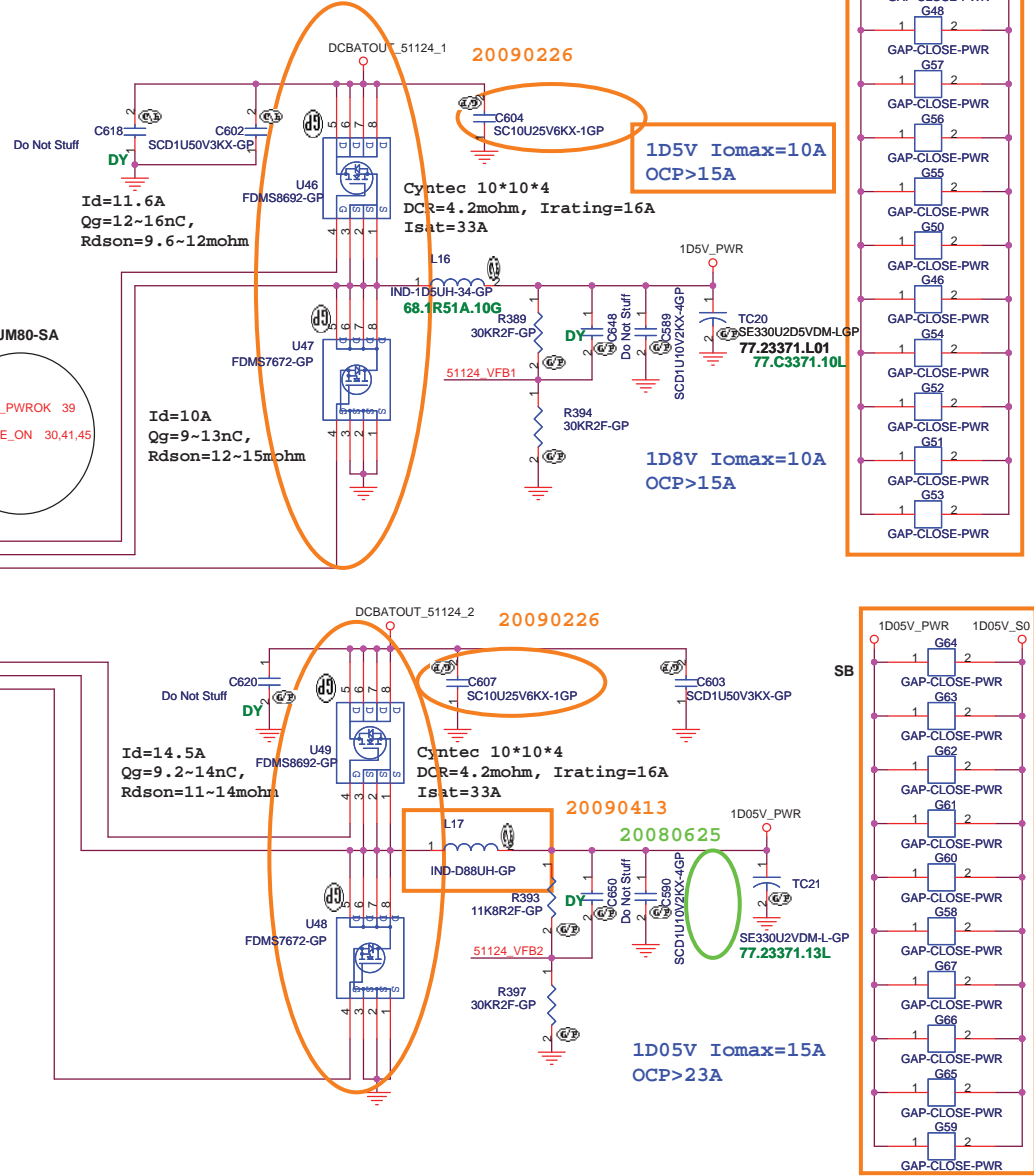
$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in}))$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode



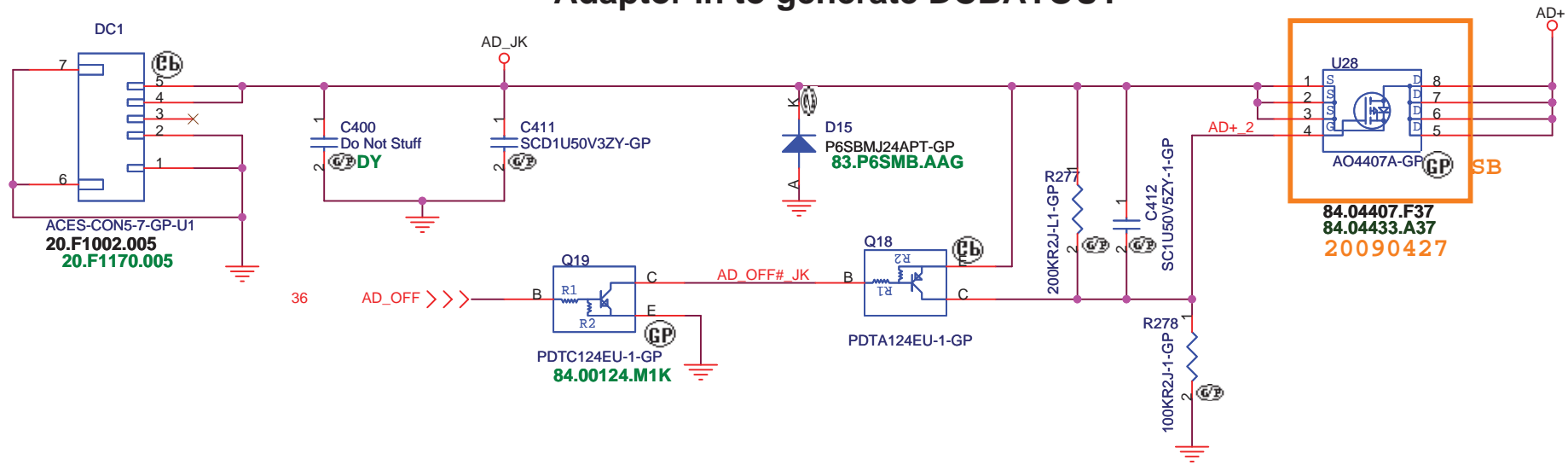
$I_d = 19.5A$
 $Q_g = 21.5 \sim 33nC$
 $R_{dson} = 5.5 \sim 6.7mohm$

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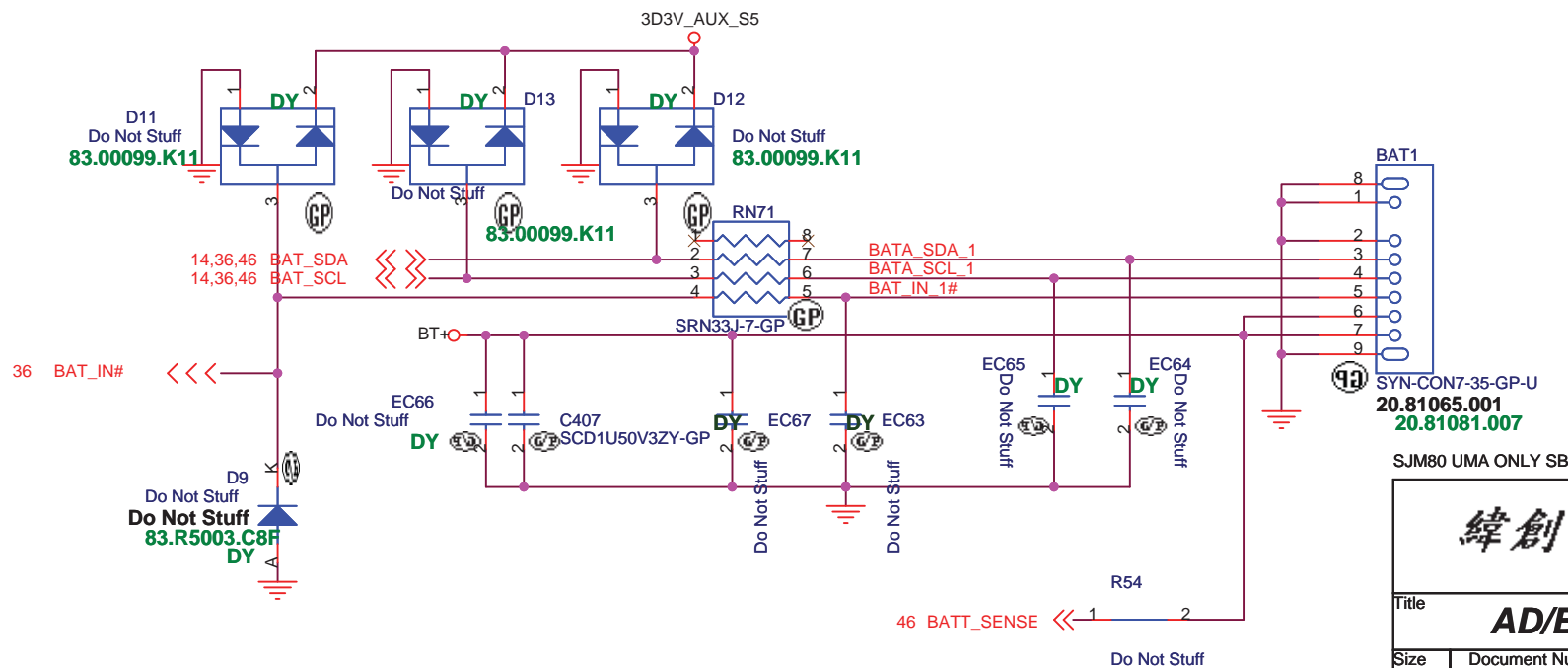
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TPS51124 1D5V 1D05V			
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Size Document Number

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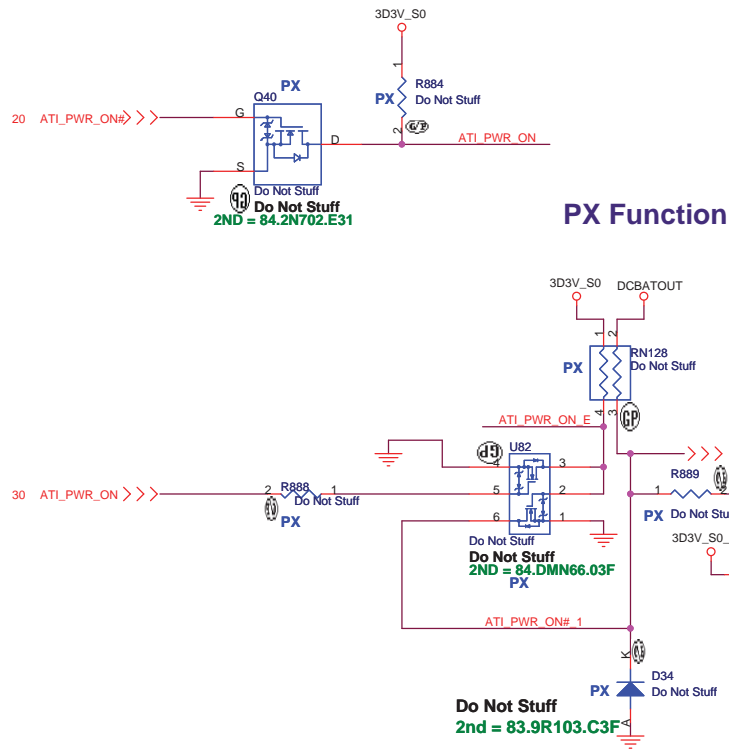
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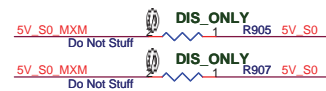
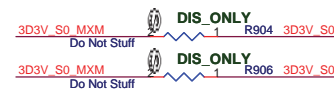
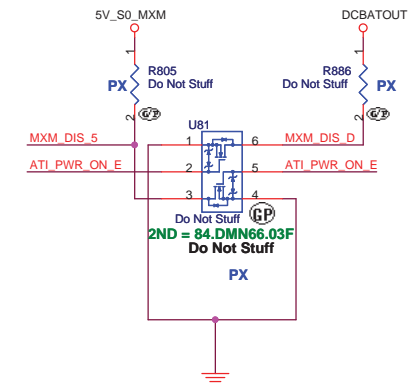
SPRING ON BOTTOM





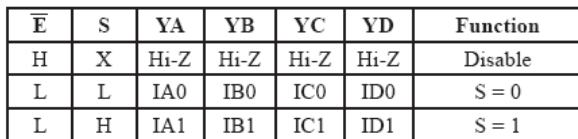
PX Function

PX Run Power Discharge circuit



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PX Run Power			
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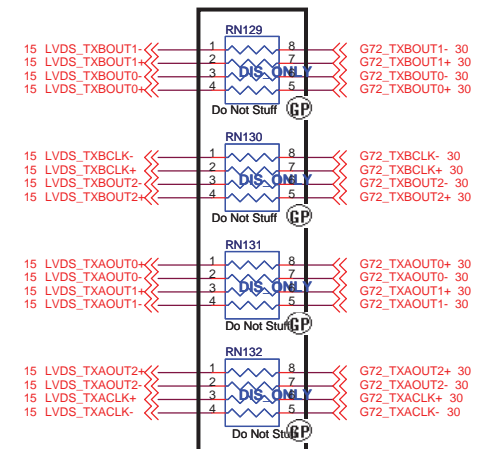
\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

PX Function



Figure 10 shows the pin connections for the SRN0J-7 4PP connector. The diagram illustrates four ICs (RN17, RN18, RN15, RN16) connected to a central vertical bus. Each IC has pins 1-4 on the left and 5-8 on the right. Red arrows indicate connections to LVDS signals, and green arrows indicate connections to GMCH signals.

IC	Pin	Signal
RN17	1	LVDS_TXBOUT0+ <--
	2	LVDS_TXBOUT0- <--
	3	LVDS_TXBOUT1+ <--
	4	LVDS_TXBOUT1- <--
	5	GMCH_TXBOUT0+ >
	6	GMCH_TXBOUT0- >
	7	GMCH_TXBOUT1+ >
	8	GMCH_TXBOUT1- >
RN18	1	LVDS_TXBOUT2+ <--
	2	LVDS_TXBOUT2- <--
	3	LVDS_TXBCLK+ <--
	4	LVDS_TXBCLK- <--
	5	GMCH_TXBOUT2+ >
	6	GMCH_TXBOUT2- >
	7	GMCH_TXBCLK+ >
	8	GMCH_TXBCLK- >
RN15	1	LVDS_TXAOUT1+ <--
	2	LVDS_TXAOUT1- <--
	3	LVDS_TXAOUT0+ <--
	4	LVDS_TXAOUT0- <--
	5	GMCH_TXAOUT1+ >
	6	GMCH_TXAOUT1- >
	7	GMCH_TXAOUT0+ >
	8	GMCH_TXAOUT0- >
RN16	1	LVDS_TXACLK+ <--
	2	LVDS_TXACLK- <--
	3	LVDS_TXAOUT2+ <--
	4	LVDS_TXAOUT2- <--
	5	GMCH_TXACLK+ >
	6	GMCH_TXACLK- >
	7	GMCH_TXAOUT2+ >
	8	GMCH_TXAOUT2- >



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SJM80 Schematic EC Tracking Record LAB 0325 , 2009
EC #/ Page / Description / Part Affected

- EC SB03/26/change R359 R360 上件(for PX function)
- EC SB03/26/change RN27 RN31 RN32 RN33 上件(for PX function)
- EC SC03/30 change REAR1,REAR2 Net name
- EC SB03/31 add digital Mic function
- EC SB04/03 change Brightness setting from NB
- EC SB04/03 modify MMB BD add switch
- EC SB04/06 Change LAN Crystal setting
- EC SB04/07 Close Power GAP
- EC SB04/07 Change PCB Version
- EC SB04/13 Keep JV80 GPIO and Function Key
- EC SB04/20 add R946 R947 for BRIGHTNESS Bypass
- EC -105/03 change C834~C841 to 0 ohm for HDMI no display design
- EC -105/03 add R948 for DIS ONLY HDP
- EC -105/03 change R823 to R824 for CRT no display
- EC -105/13 change MXM Card Stand off part number
- EC -105/19 MMBCN1 power 3D3V change 5V (for MMB LED light display)
- EC -105/19 Modify HDMI hot plug schematic Location Q46
- EC -105/20 change R316 to 22R2 (For USB eye diagram)
- EC -105/20 change R398 6.5k to 7.1K increase 3.3V to 3.4V
- EC -105/21 Q46 HDMI hot plug change power 3D3V_S0_MXM to 5V_S0
- EC -105/22 add Cap for EMI at CRT RGB

EC -1 01/20/Change R316 to 22D6R2F(For USB eye diagram)

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Title		
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